



## 4080 Product

Arbitrary Waveform Generator (AWG)

Capabilities and Applications

December 8, 2022

Innovation for the Next Generation

Confidential and Proprietary: Shared under NDA

# 4080 Product

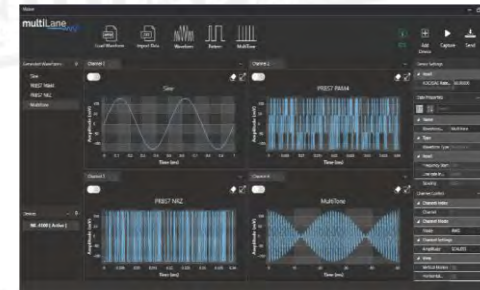
## Target applications

- High-speed SerDes, transceivers, and amplifier validation
- Receiver jitter and noise tolerance testing
- General time domain measurements of high-speed digital communication signals
- Support for compliance PHY and protocol stress testing of MIPI C/D-PHY, MIPI M-PHY, PCIe5, USB4 and others
- Coherent 400ZR module development and validation
- BER and FER tester

# 4080 Product

## Key features and instrument capabilities

- 4-channel Differential AWG (0.1-64 GB) and User Defined Modulation
- Programmable RJ and SJ (dual tones) Jitter injection in AWG mode
- Cross talk emulation by BUJ jitter injection
- ISI emulation (LPF) and de-emphasis in AWG mode
- 2 Dual-Channel (I/Q) Differential PPG (25-64 GB) with NRZ/PAM4 modulation
- Coherent signals generation for QAM modulation
- Built-in 7-tap or 60-tap FFE in PPG mode



# 4080 Product

## Electrical Specifications

Parameter	Specifications
TX Coupling	AC coupled
Channel Impedance (Diff)	100 Ohm
TX/RX connectors	SMPM (M)
TX 3dB Bandwidth	35 GHz
Reference clock Output	Baud Rate/48 or Baud Rate/24 (<1.2GHz max)
Clock out amplitude (SE/Diff)	0.6/1.2 Vpp
Clock input amplitude (SE/Diff)	0.5/1 Vpp
Clock Input Validated Range	150 - 160 MHz
Instrument Automatic Shutoff	85 °C
Recovery from over-temperature shutoff	Manual reboot of the system and instrument temperature below 85 °C
Setup time / Reboot	38 s
Normal Operating Temperature	0 - 65 °C
Power	12 V, 1.5 A



# 4080 Product

## Arbitrary Waveform Generator specifications

Parameter	Specifications
Tx Maximum Amplitude (Sine wave)	1050 mVppd
Bit Rates	1 – 64 Gbps
Vertical Resolution	8 bits
Modulation	User-defined
Pre-programmed Waveforms	PRBS 7, PRBS 9, Square wave, triangular Wave, sinewave, multi-tone, linear chirp, log chirp, sawtooth, exponential rise, exponential decay, Sinc, Lorentz, Surge, Damped Oscillation, Stairs, Serial Data, half-sine, Distorted sinewave and Gaussian.
Memory Depth	33.6 kSa per channel

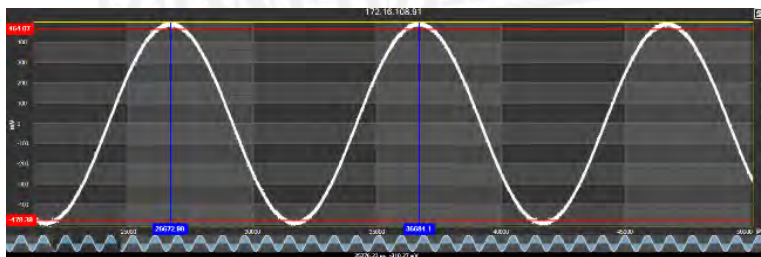
# 4080 Product

## Pulse Pattern Generator specifications

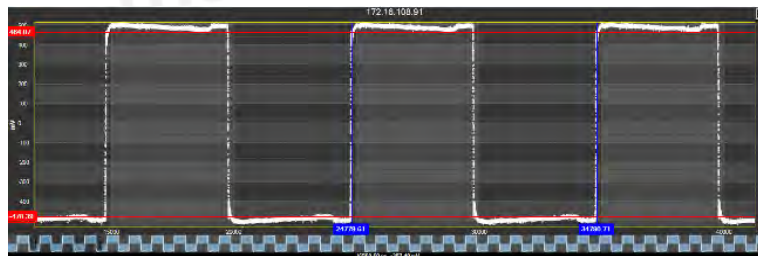
Parameter	Specifications
Bit Rates	25 – 64 GBd
Modulation	NRZ and PAM4
Tx Maximum Amplitude at 26G	750 mVppd (350 mVppd in calibration mode)
Tx Maximum Amplitude at 53G	500 mVppd (300 mVppd in calibration mode)
Patterns	PRBS 7/9/11/15/20/23/29/31/35/39/41/47
TX Amplitude Adjustment	Steps of 1 mV
TX Equalization	FFE 3 taps or 7 taps
Pre-Emphasis Resolution	±168 steps
Equalizing Filter Spacing	1UI

# 4080 Product – AWG Examples

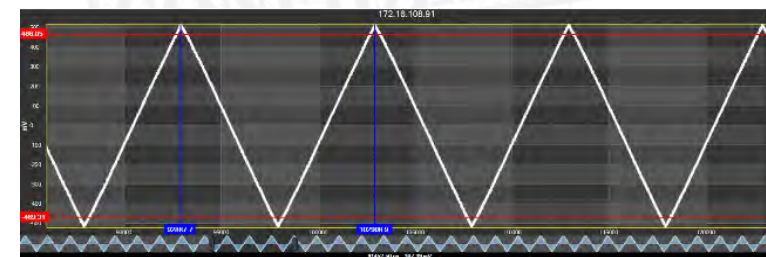
Sine



Square



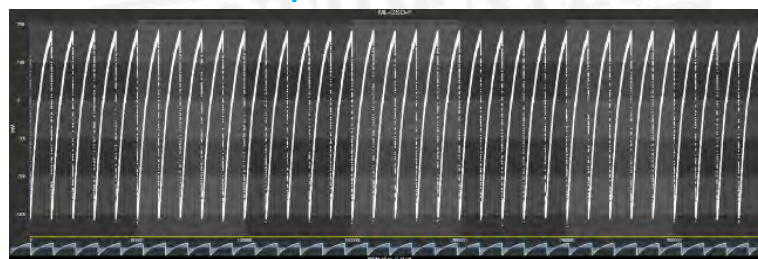
Triangular



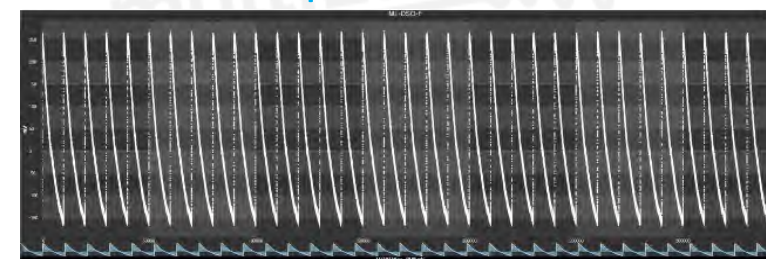
Saw Tooth



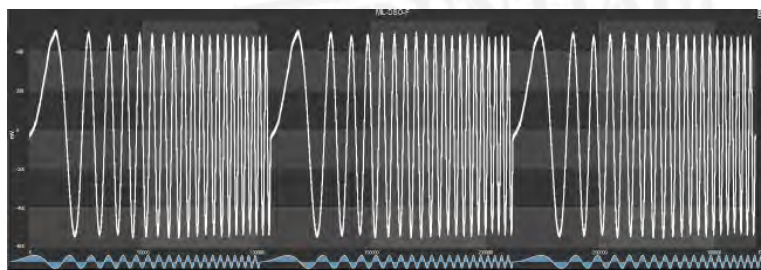
Exponential Rise



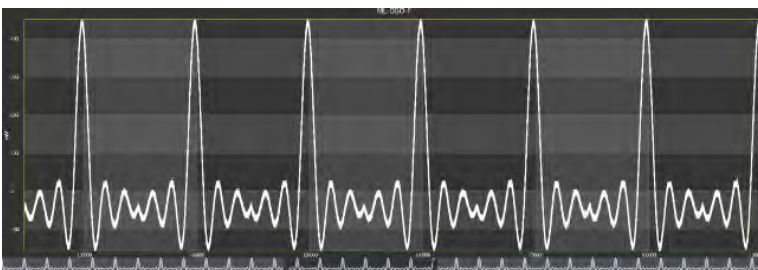
Exponential Fall



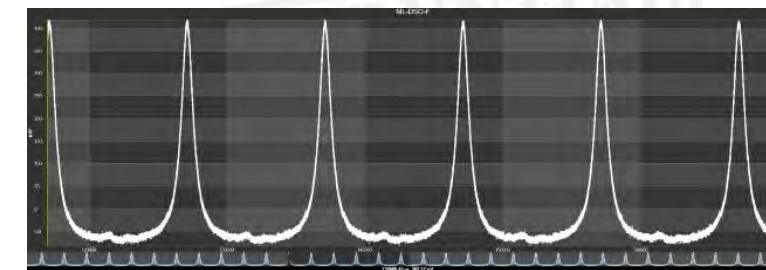
Linear Chirp



Sinc



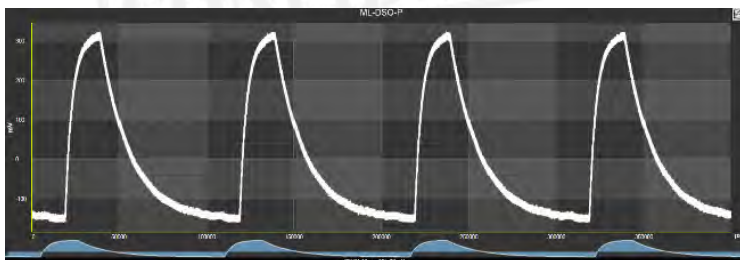
Lorentz



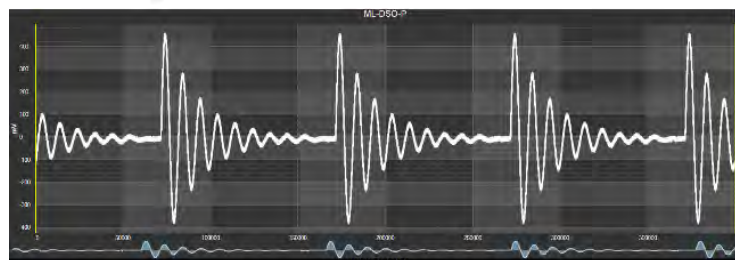


# 4080 Product – AWG Examples

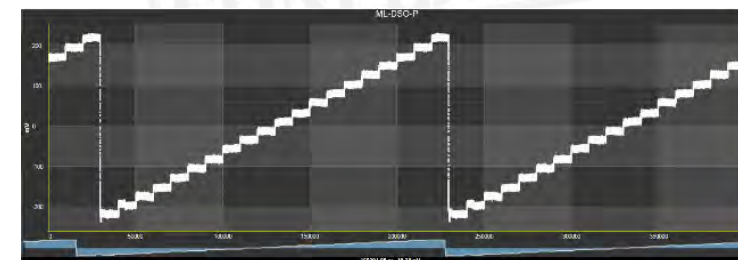
Surge



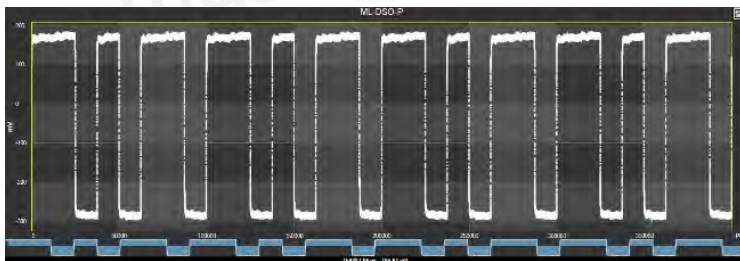
Damped Oscillation



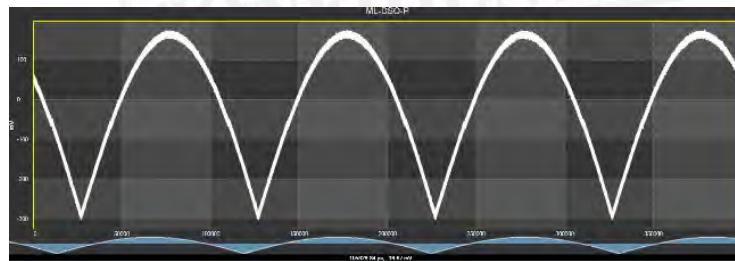
Stairs



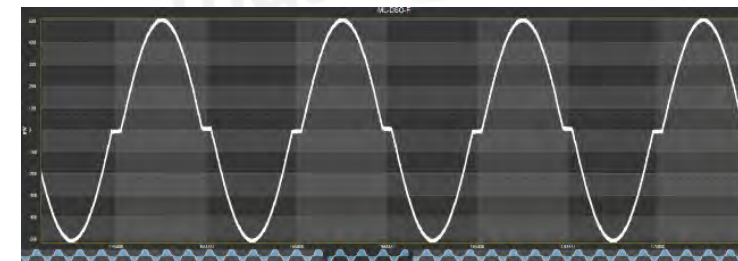
Serial Data



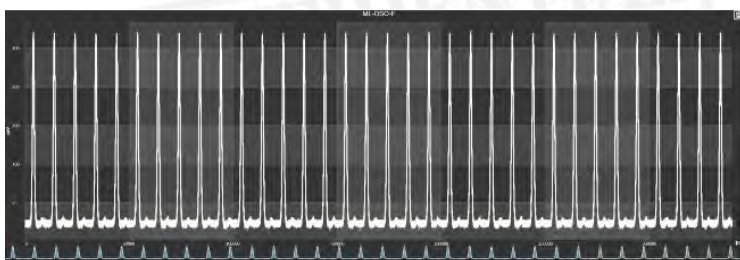
Half Sine Wave



Distorted Sine Wave



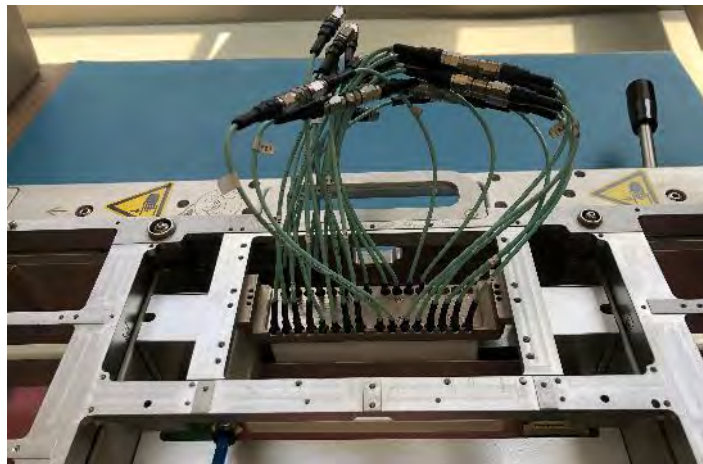
Gaussian



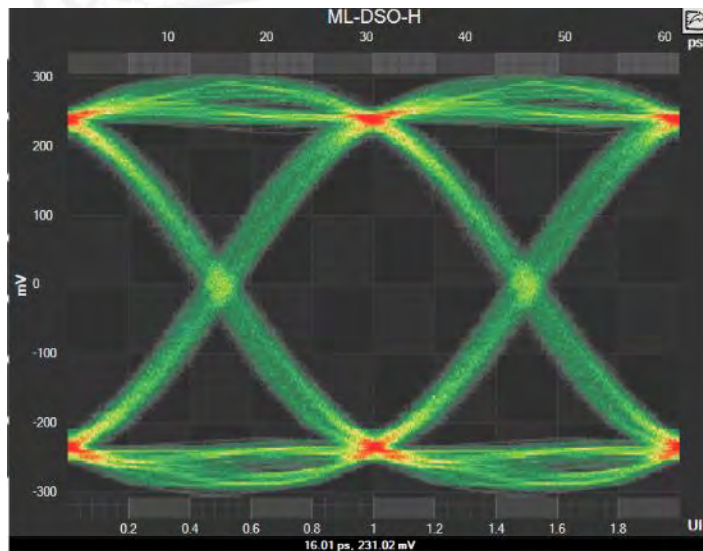
# Applications Examples

- USB 4.0 (NRZ, 20 Gbps)
- USB 4.1 (PAM3, 25.6 GBd)
- PCIe gen5 (NRZ, 32.5 Gbps)
- PCIe gen6 (PAM4, 32.5 GBd)
- ThunderBolt
- Ethernet 112G/Lane

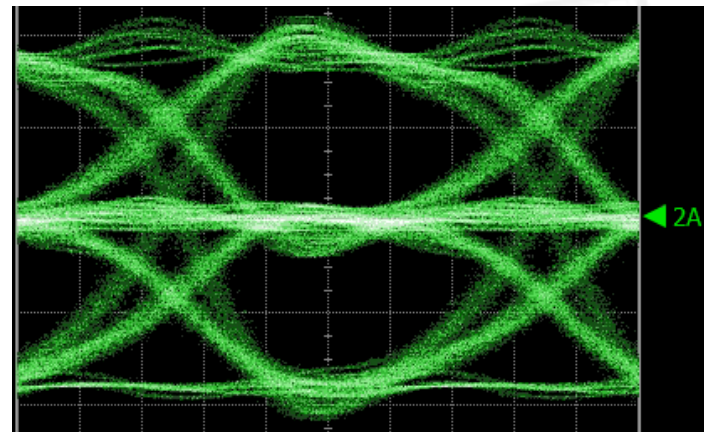
Setup



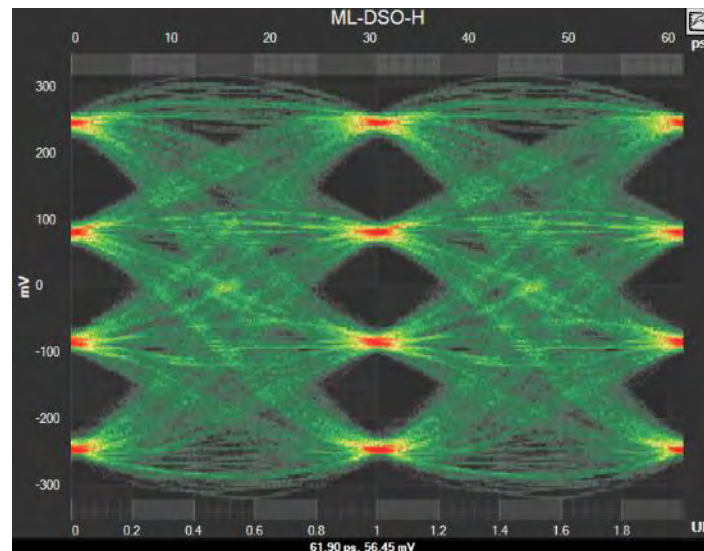
32.5G NRZ Signal



26 GBd PAM3 Signal



32.5G PAM4 Signal





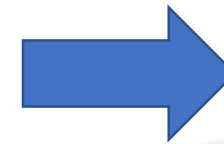
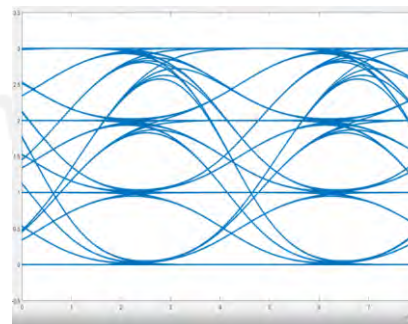
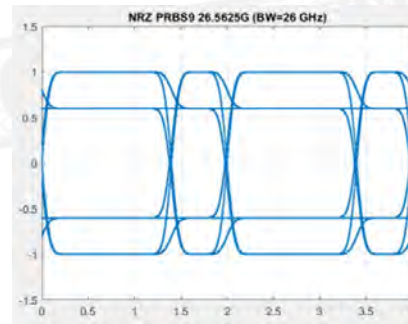
# PAM4 Editor

## Reshaping PAM4 Signal

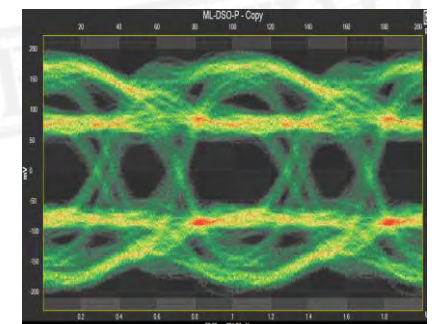
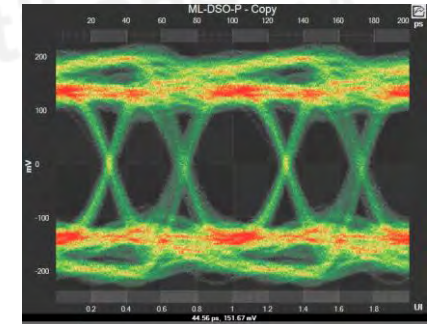
Ability to reshape PAM4 signal using AWG, with the following:

- Level mismatch ratio (RLM)
- Duty cycle distortion
- Amplitude
- Rise time
- Fall time

### Simulation



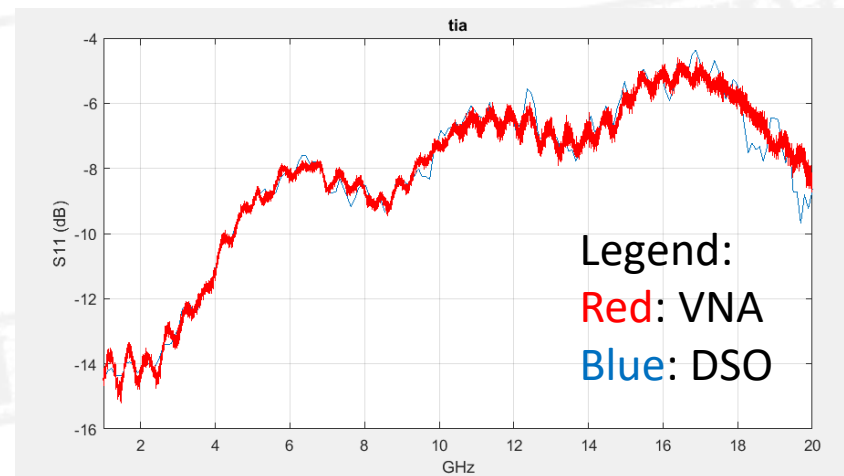
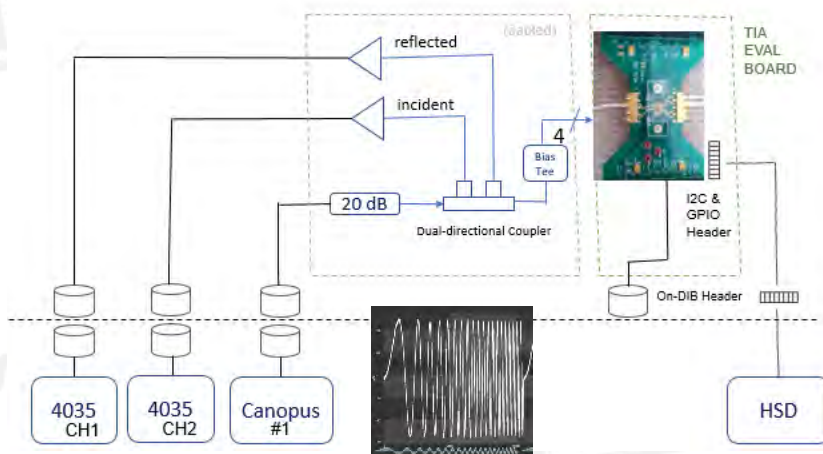
### DSO



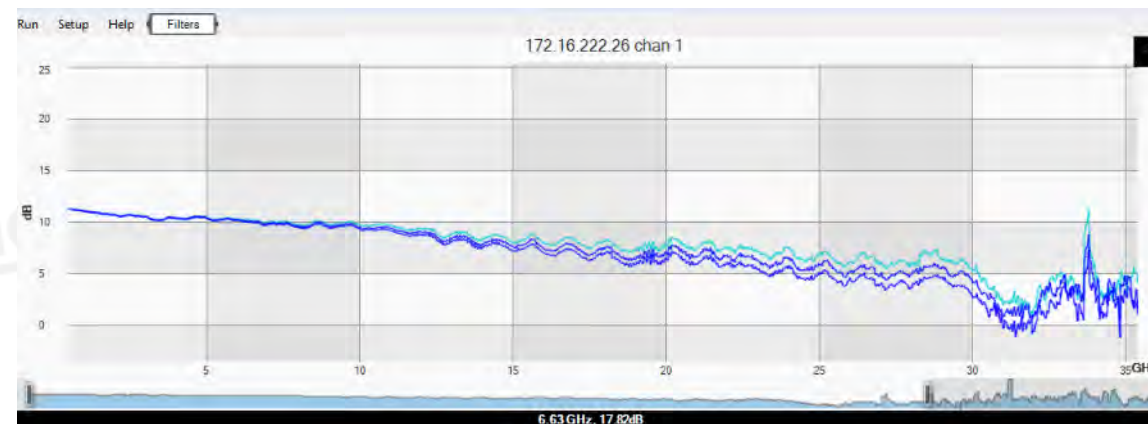
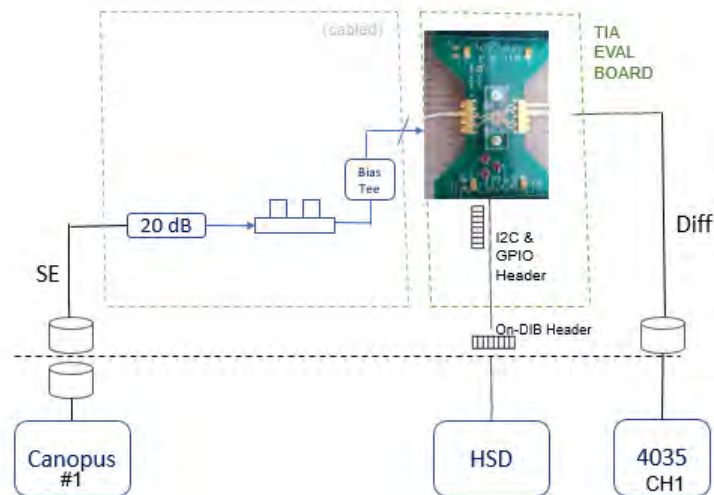


# S11 and S21 using 4080

- S11: Canopus source with Chirp function and directional couplers



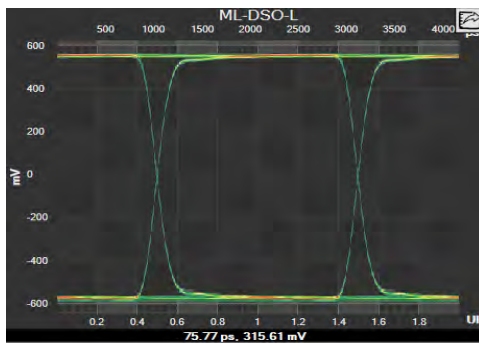
- S21: amplifier bandwidth vs peaking



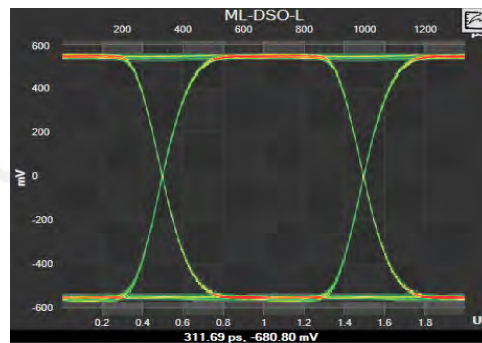
# 4080 Product

## Compliance Test Patterns – PRBS7 patterns generated in AWG mode

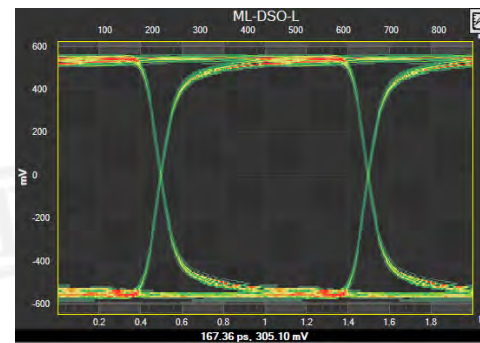
PRBS7 NRZ at 480 Mbps



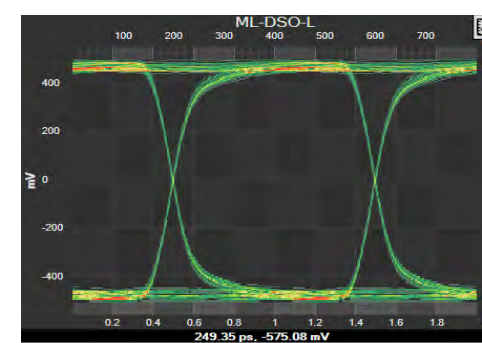
PRBS7 NRZ at 1.5 Gbps



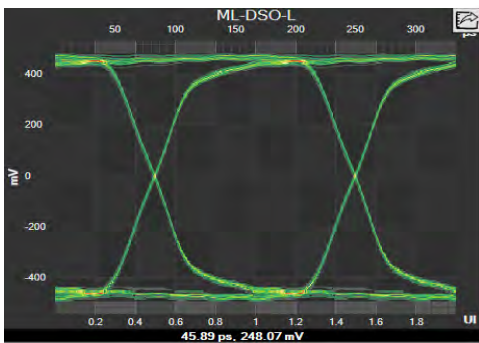
PRBS7 NRZ at 2.3 Gbps



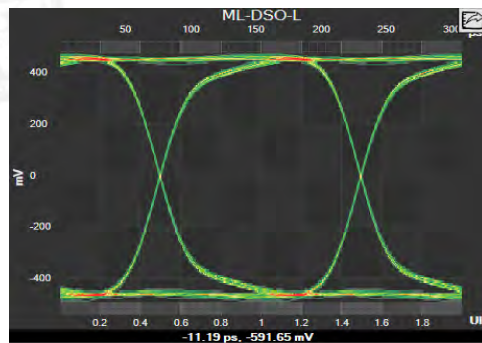
PRBS7 NRZ at 2.5 Gbps



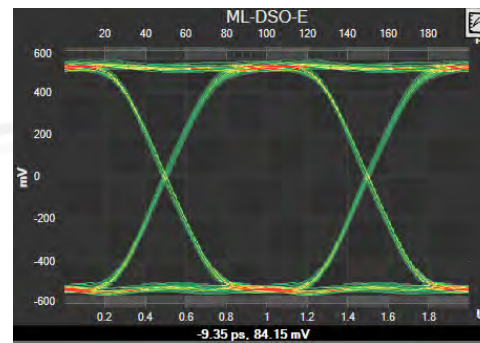
PRBS7 NRZ at 6 Gbps



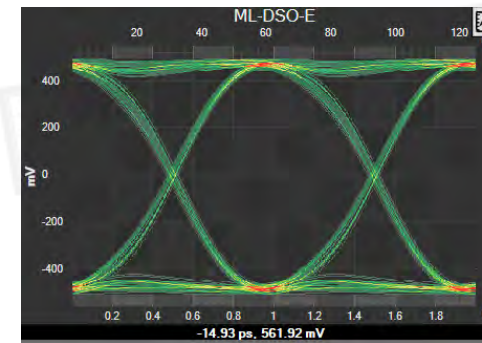
PRBS7 NRZ at 6.5 Gbps



PRBS7 NRZ at 10 Gbps



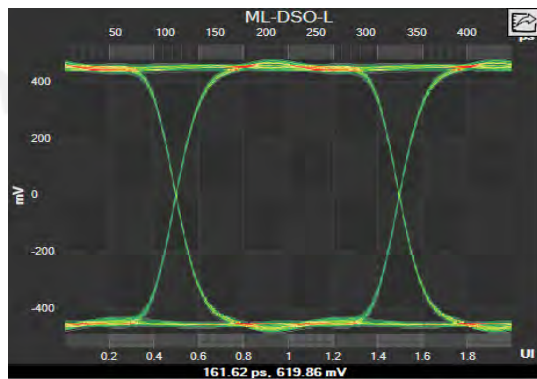
PRBS7 NRZ at 16 Gbps



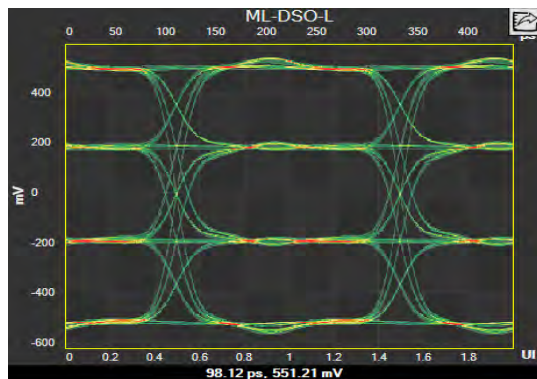
# 4080 Product

## MIPI C-PHY Compliance Test Patterns

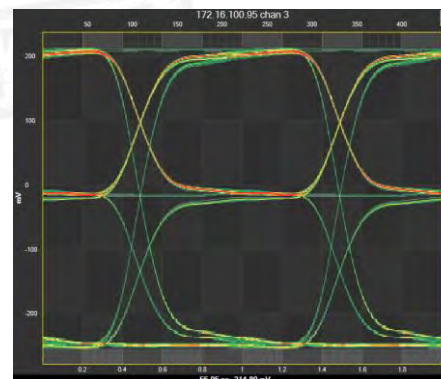
PRBS7 NRZ at 4.5 Gbps



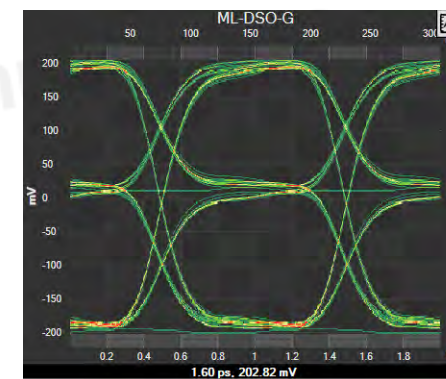
PRBS7 PAM4 at 4.5GS/s



MIPI C-PHY 3-level signaling at 4.5 GS/s



MIPI C-PHY 3-level signaling at 6.5 GS/s

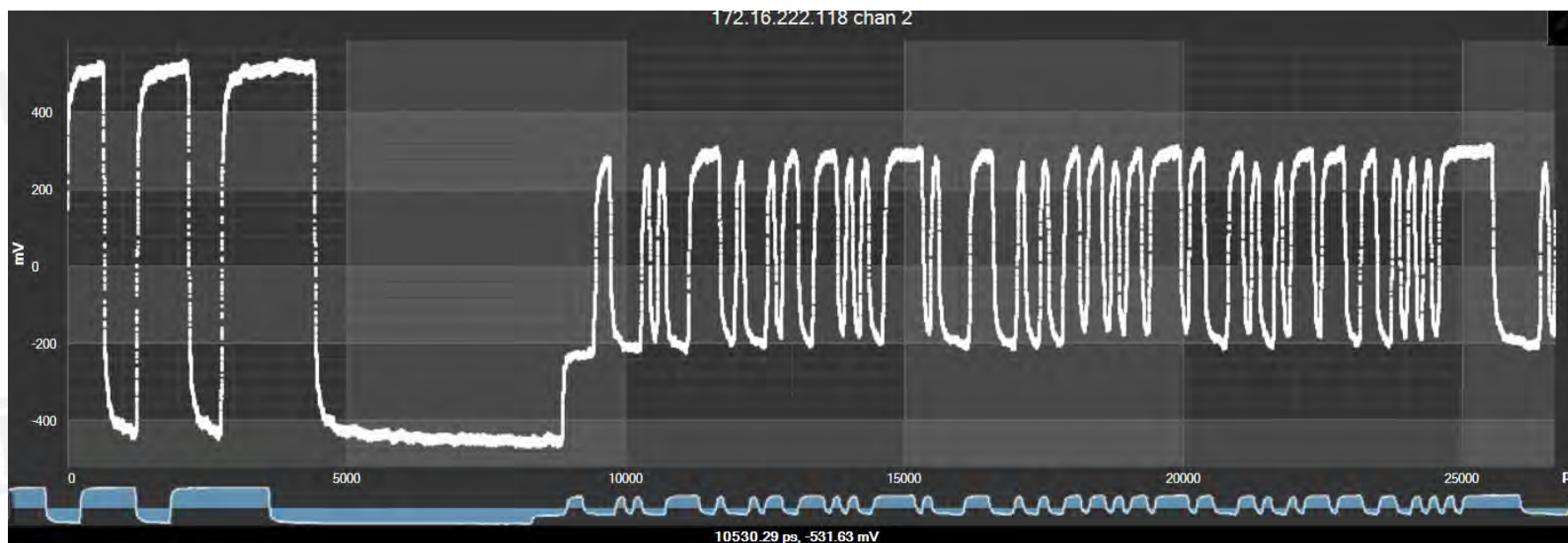




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## MIPI C-PHY/D-PHY Compliance Testing

Generation of LP (Low Power) and HS (High Speed) signals in AWG mode

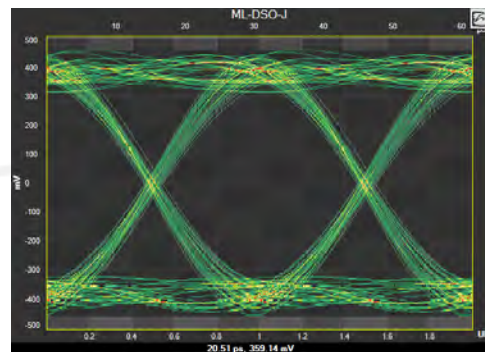


Example of HS PRBS7 at 7.14375 GS/s with LP square wave

# 4080 Product

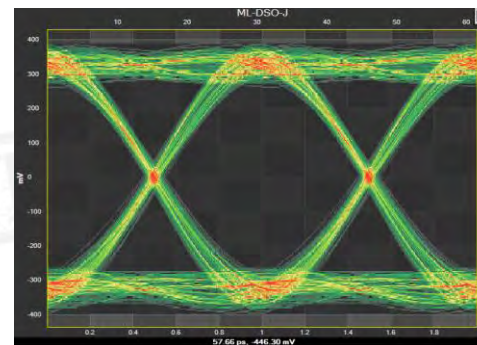
PCIe Gen5 and Gen6 PRBS Patterns – NRZ and PAM4 at 32 GS/s

PRBS7

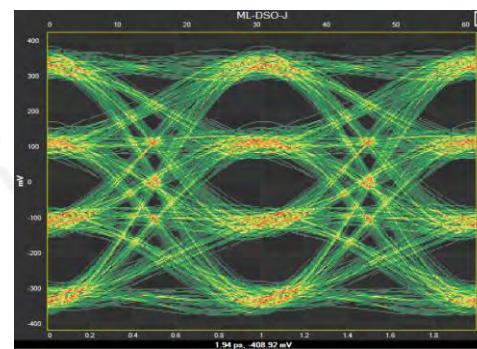
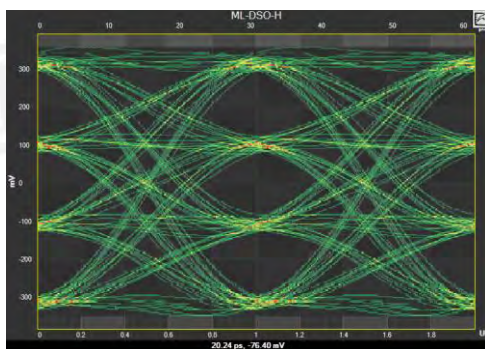


NRZ

PRBS9

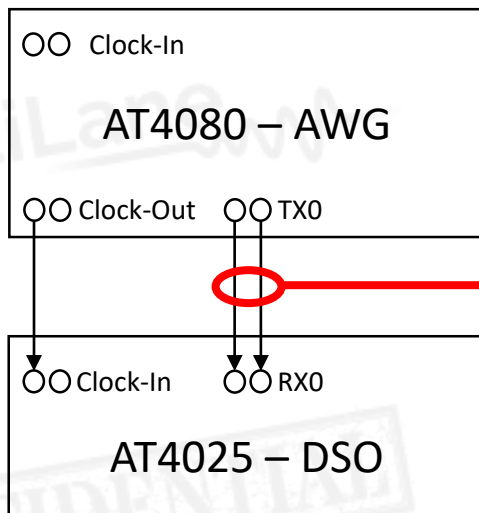


PAM4

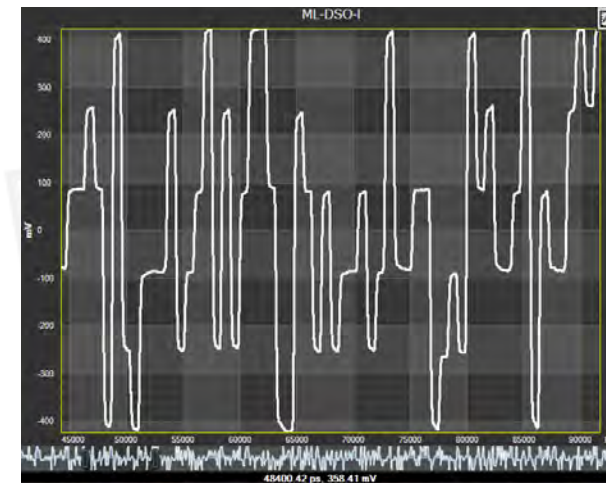
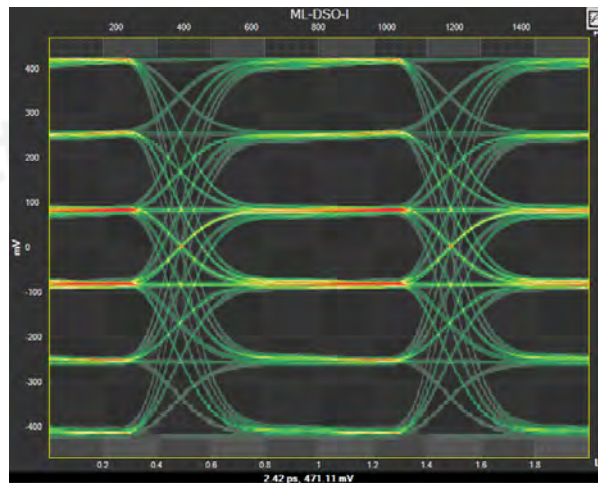


# 4080 Product

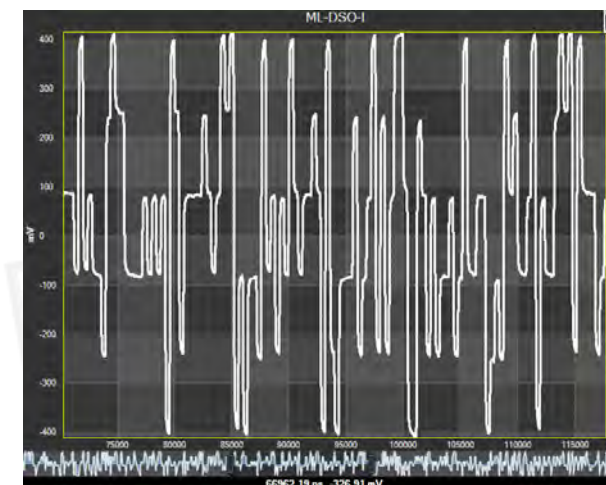
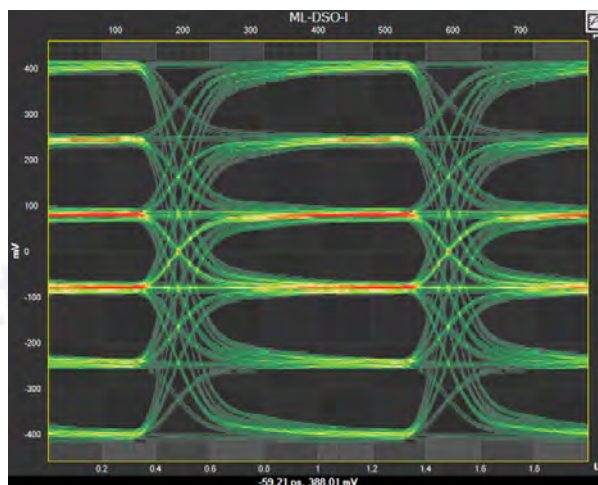
## PAM6 Generation in PPG mode



At 1.25 GHz



At 2.5 GHz



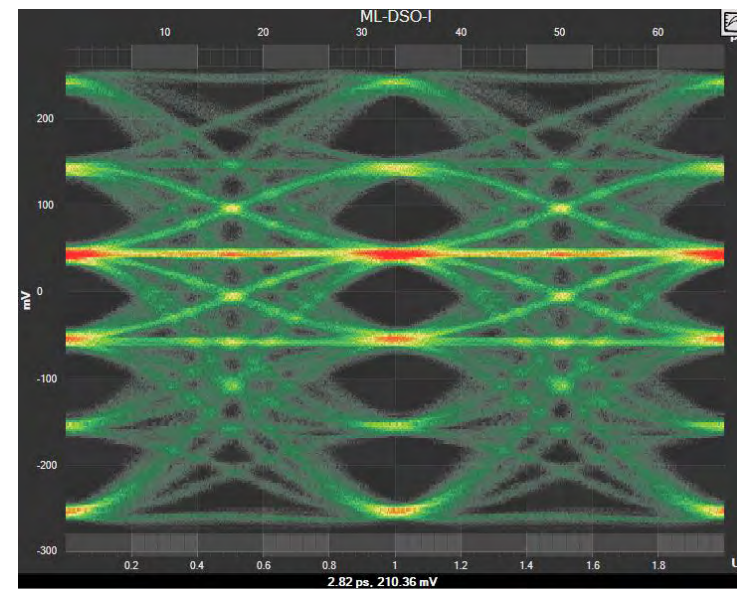
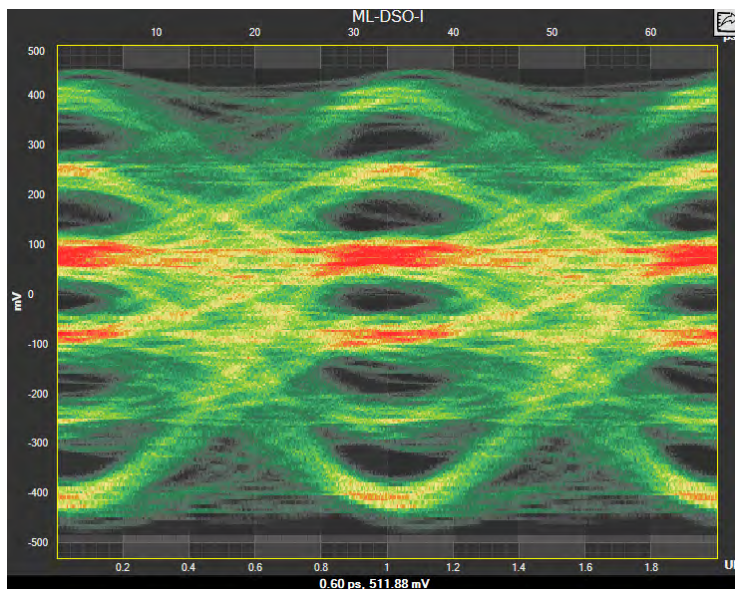
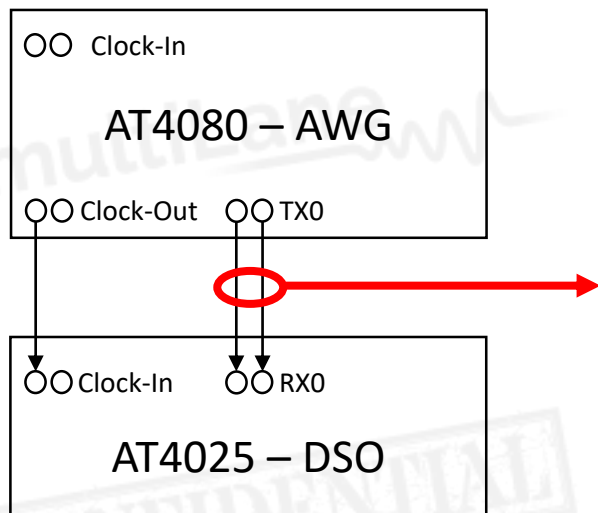


# 4080 Product

PAM6 Generation in PPG mode **At 30 GHz**

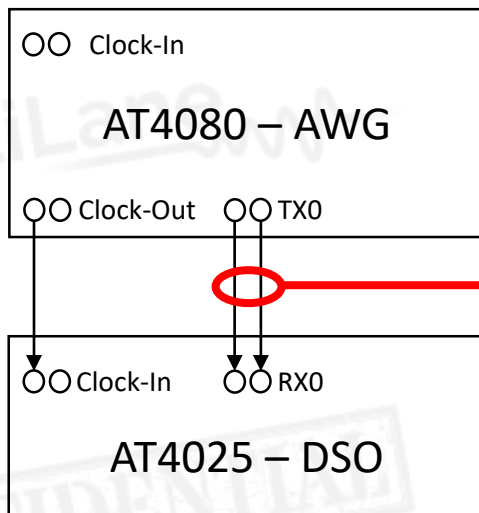
Without Pre-Equalization

With Pre-Equalization

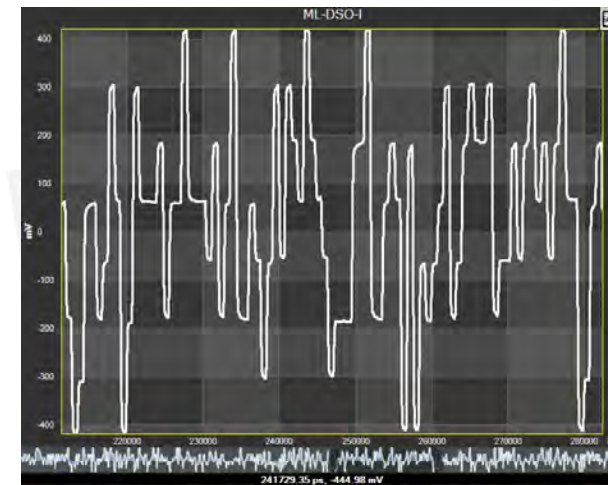
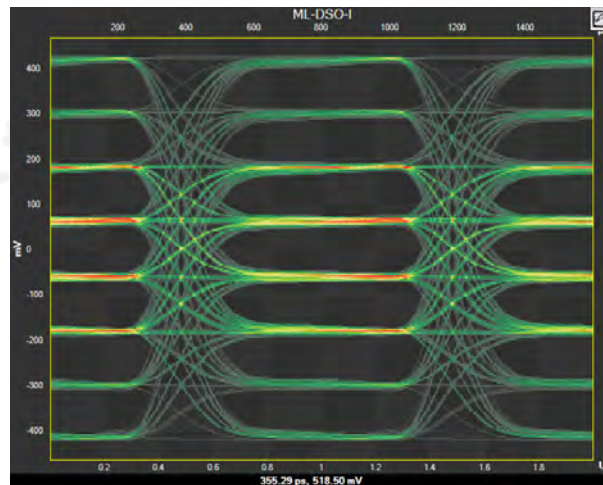


# 4080 Product

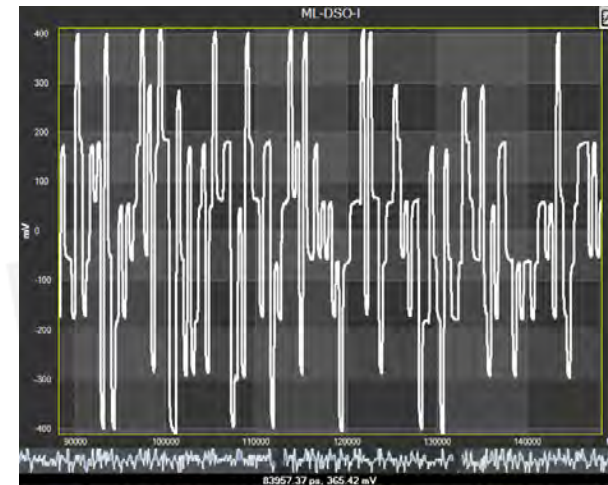
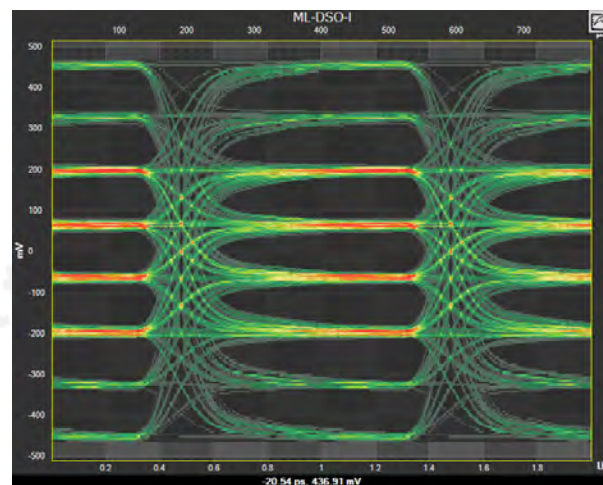
## PAM8 Generation in PPG mode



At 1.25 GHz



At 2.5 GHz



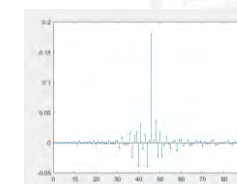
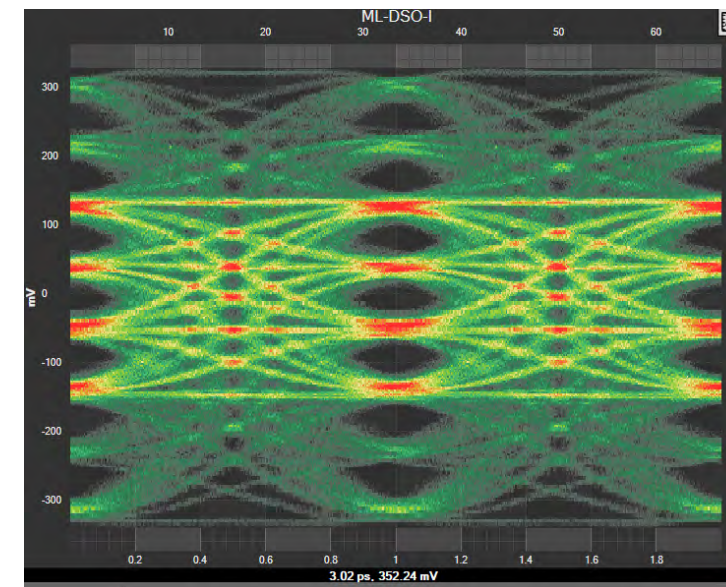
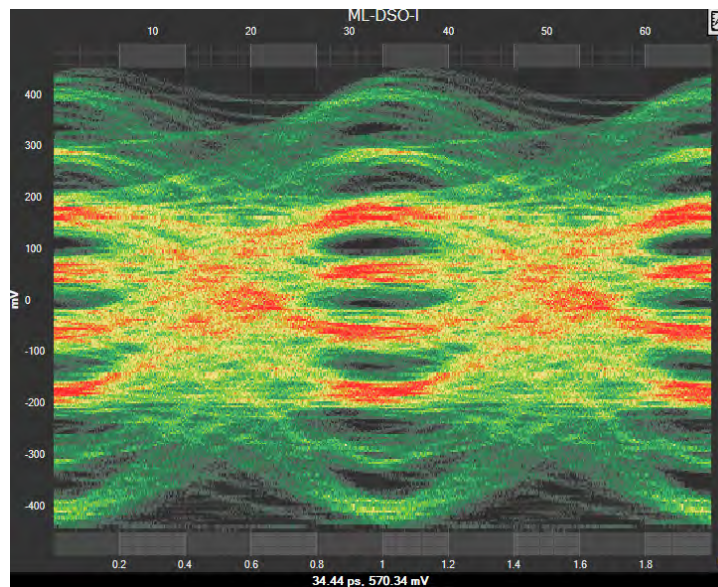
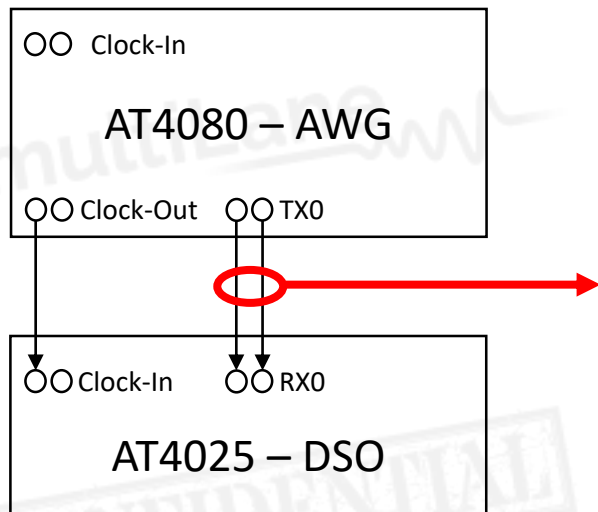


# 4080 Product

PAM8 Generation in PPG mode **At 30 GHz**

Without Pre-Equalization

With Pre-Equalization



Custom FFE applied  
FIR 90 taps - 3 taps per UI

# 4080 Product – Product Capabilities and Applications

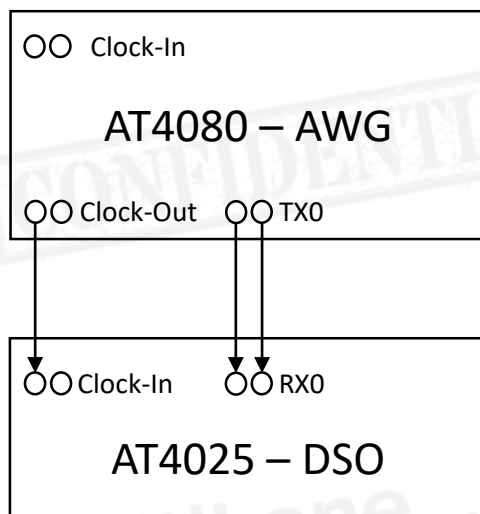
## Compliance Test Patterns Generation for PCIe Gen 3 and 4

### 4080 Product Capabilities for PHY compliance and stressed Eye testing

- Random Jitter (RJ) injection by software
- Sinusoidal Jitter (SJ) injection by software (both single and dual tones options)
- Inter-Symbol Interference (ISI) emulation by software
- Cross-talk emulation by Bounded Uncorrelated Jitter (BUJ) injection by software
- De-embedding s-parameters by applying customized patterns after pre-processing
- Spread-Spectrum Clocking supported for PCIe compliance testing

# Jitter Measurements – PRBS 11

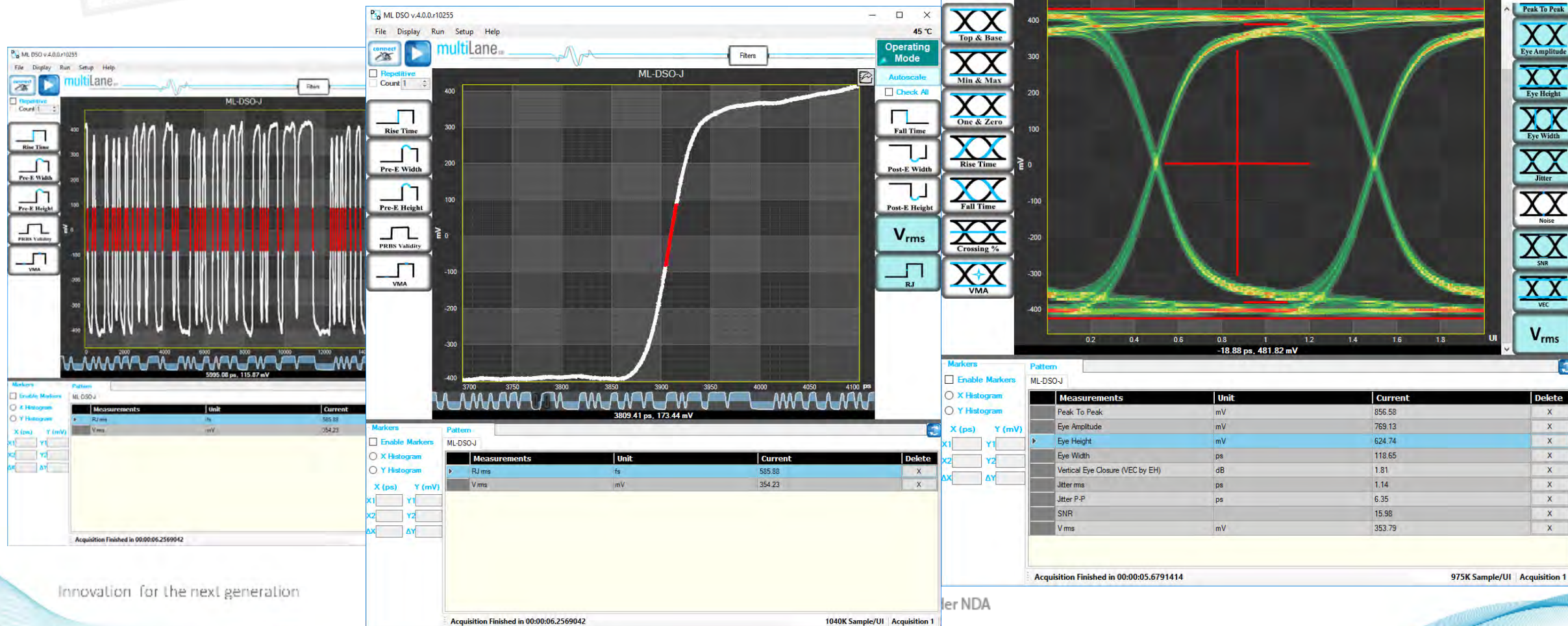
Single tone Jitter injection by software for PCIe Gen 3 and Gen 4





# PCIe Gen3 8Gbps - Jitter Measurements

PRBS7 – No jitter injection

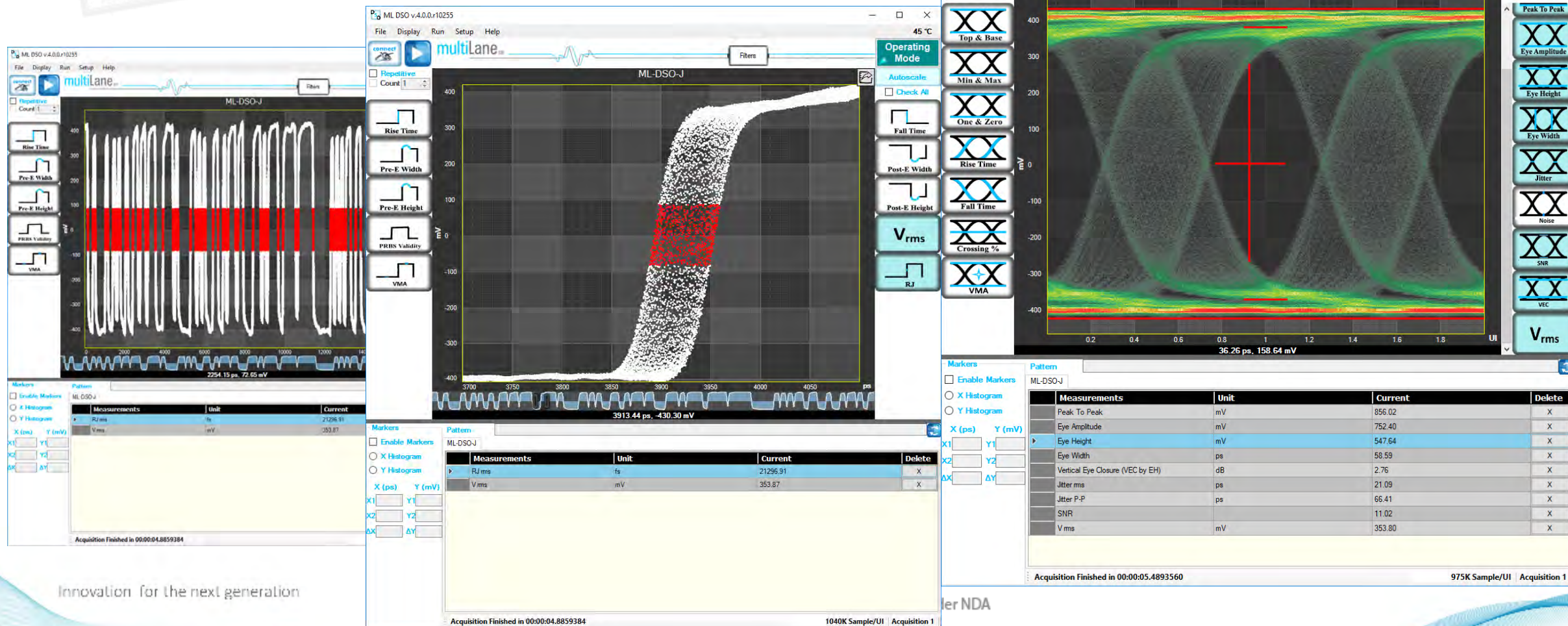




# PCIe Gen3 8Gbps - Jitter Measurements

Jitter injected by software (60 ps)

PRBS7 – Signal generated with SJ Jitter insertion at ~2 MHz





# PCIe Gen3 8Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~2 MHz

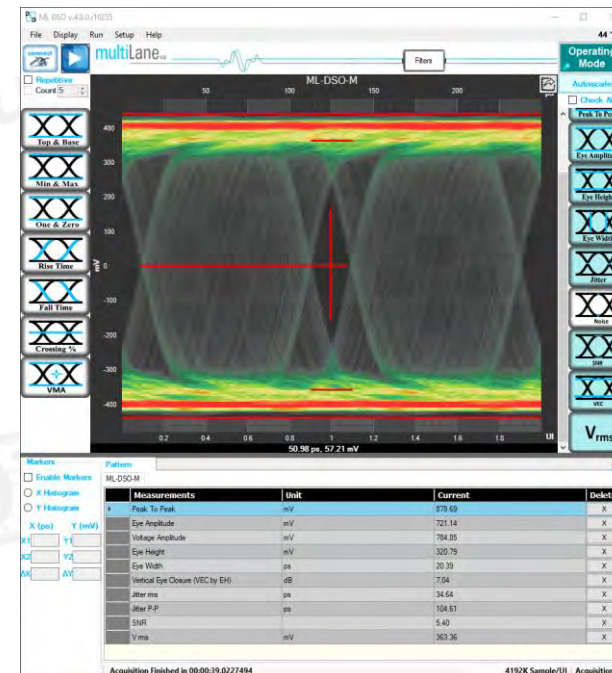
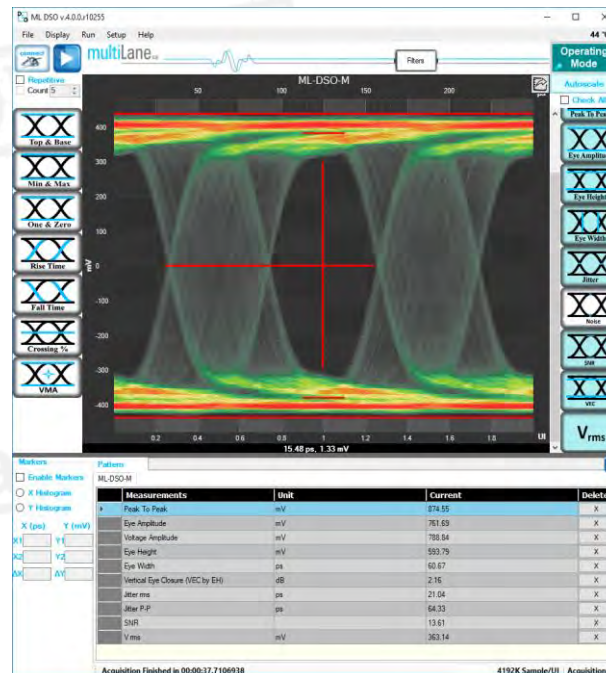
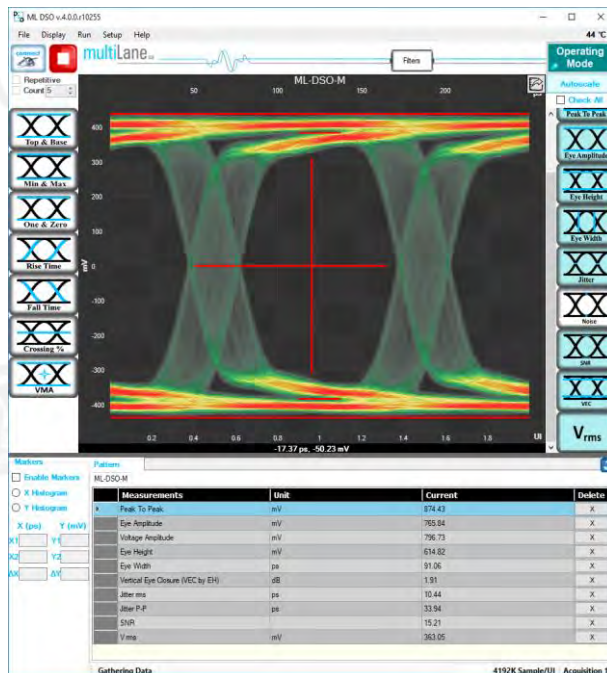
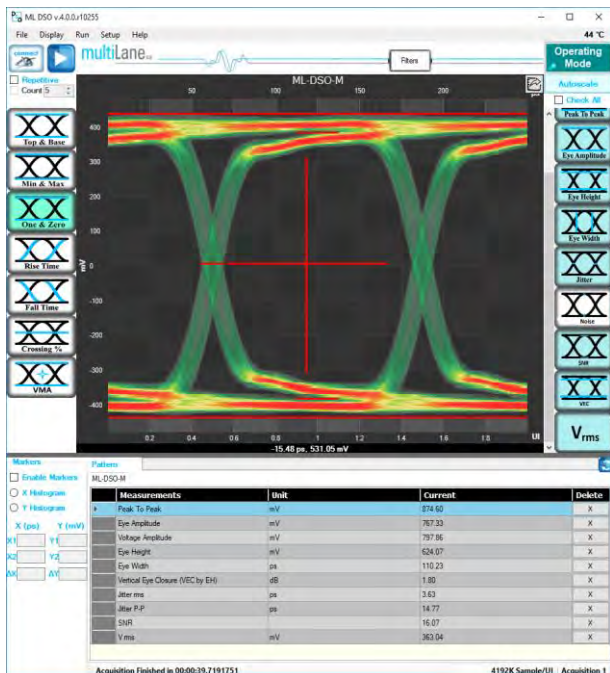
Jitter injected by software

10 ps

30 ps

60 ps

100 ps



# PCIe Gen3 8Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~10 MHz

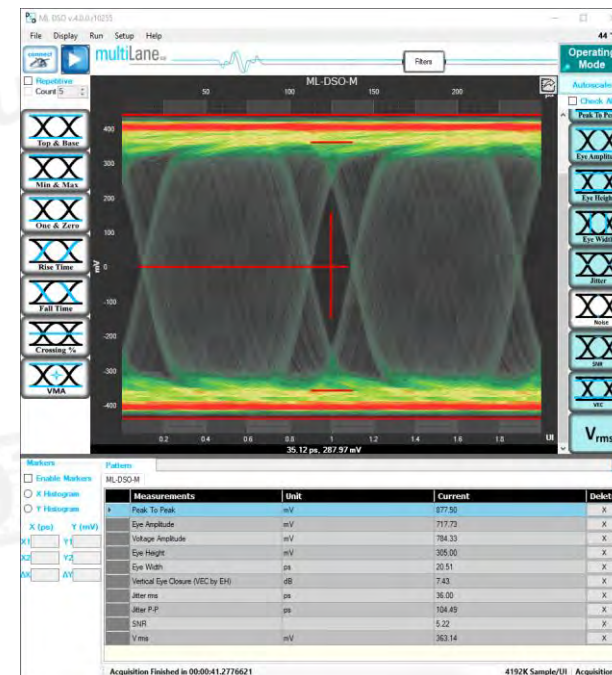
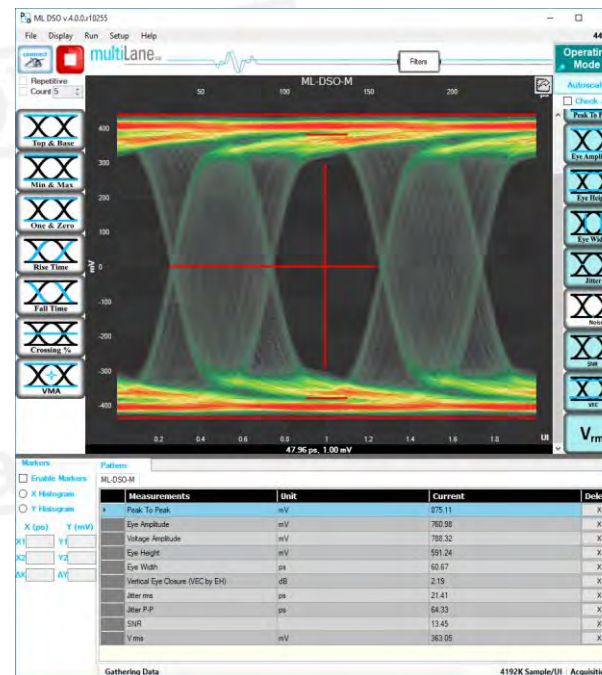
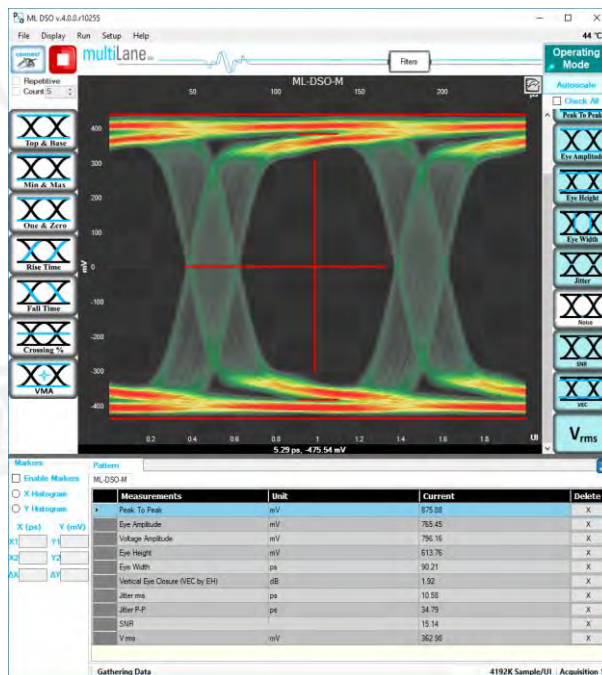
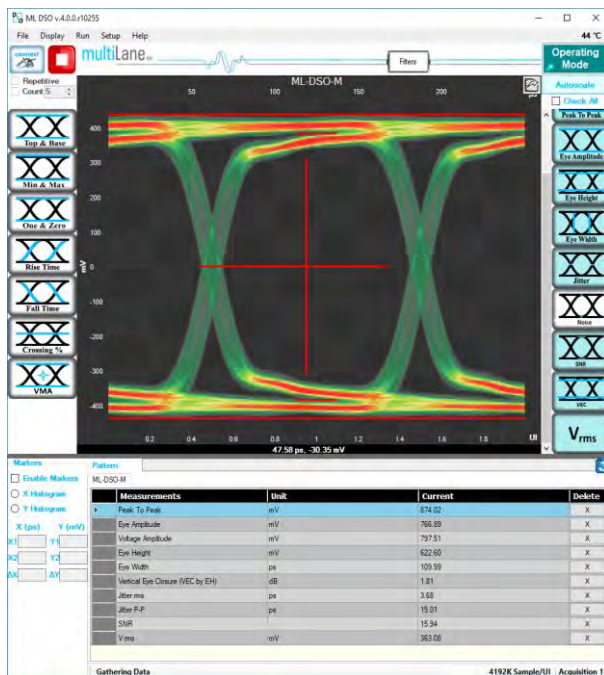
Jitter injected by software

10 ps

30 ps

60 ps

100 ps





# PCIe Gen3 8Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~100 MHz

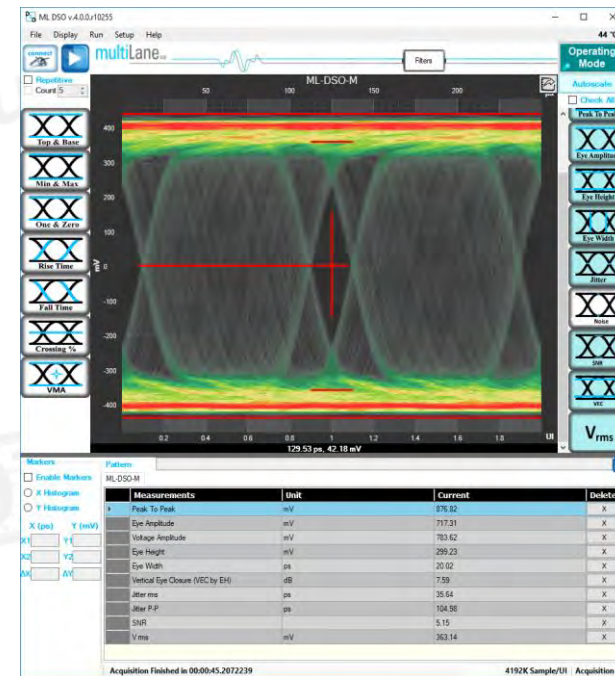
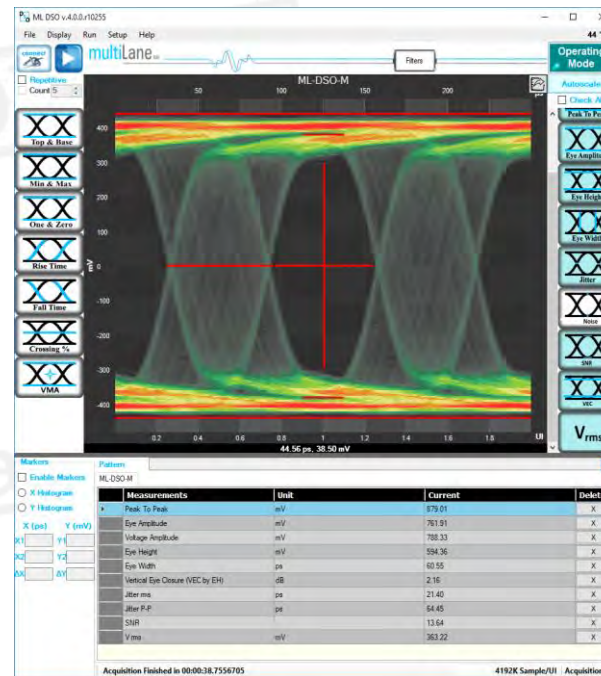
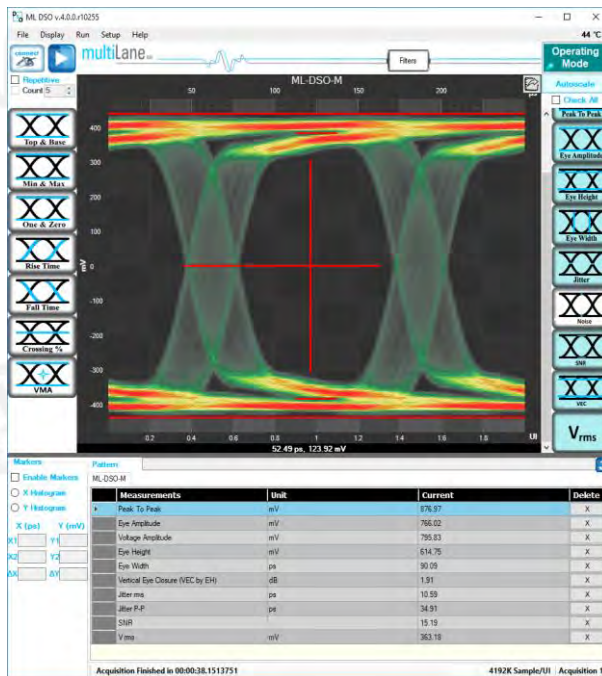
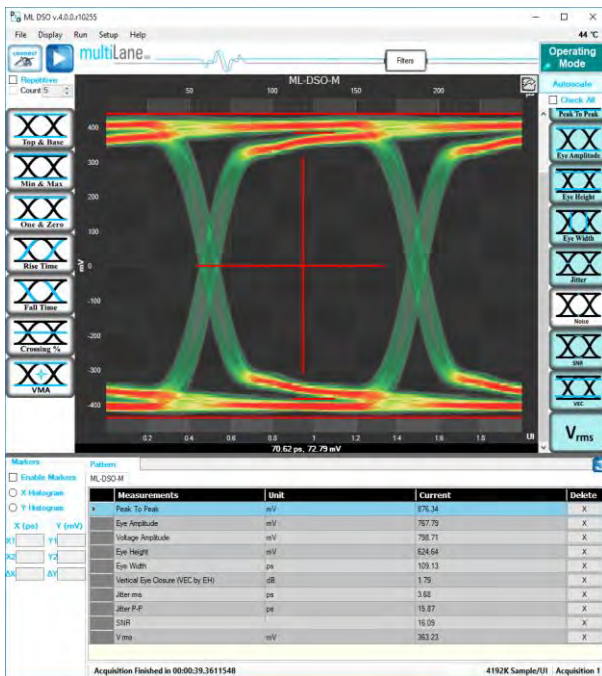
Jitter injected by software

10 ps

30 ps

60 ps

100 ps

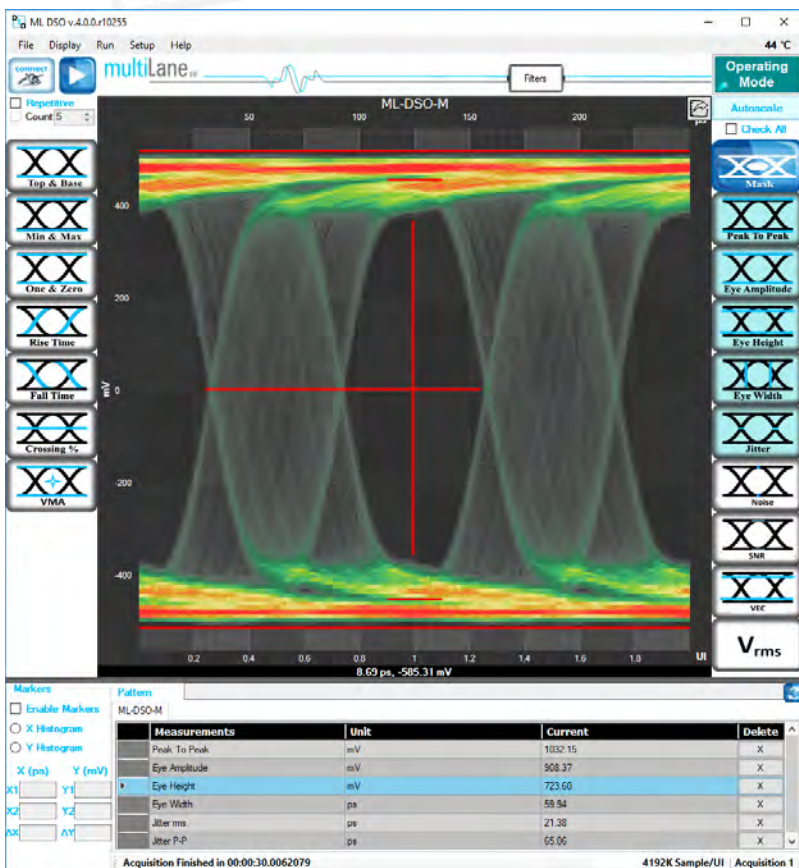




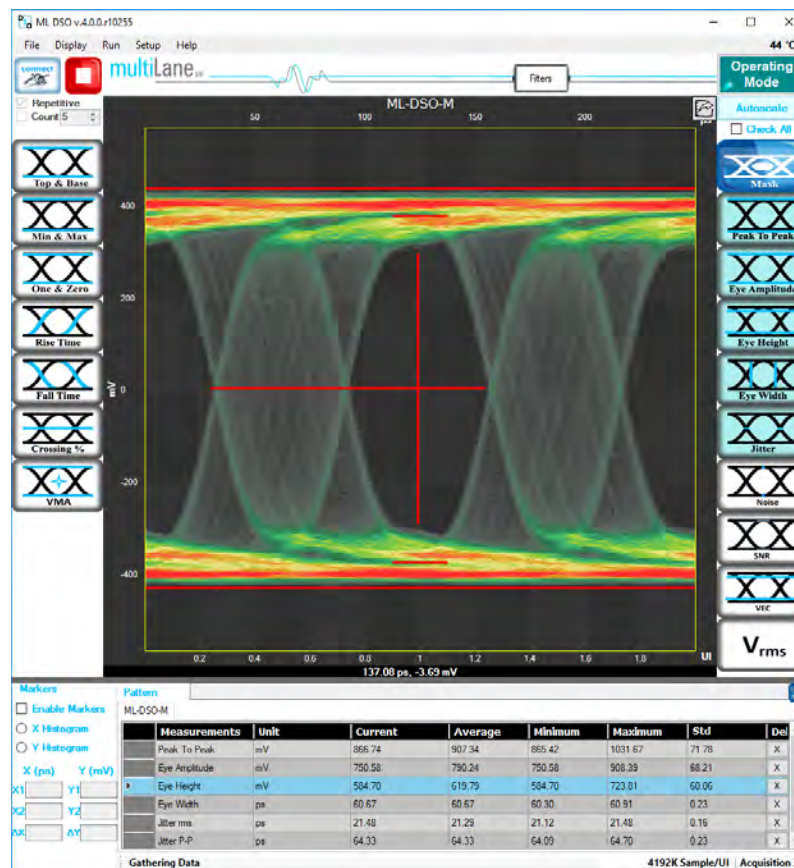
# PCIe Gen3 8Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~100 MHz (60 ps) with **Amplitude Control**

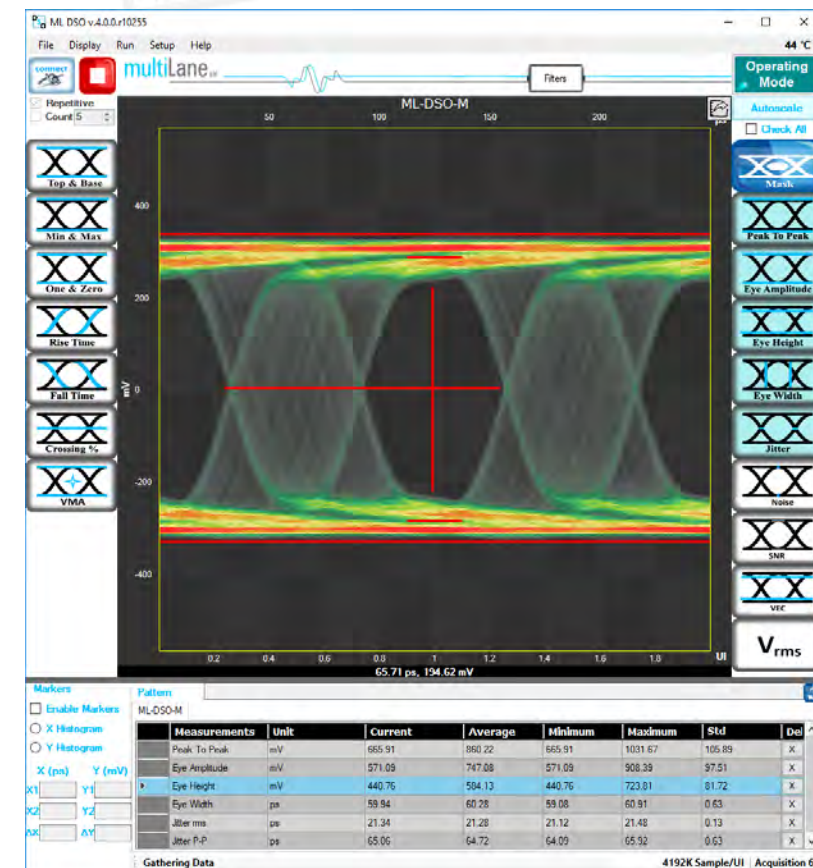
100%



80%



60%





# PCIe Gen4 16Gbps - Jitter Measurements

PRBS7 – No jitter injection

The image displays three screenshots of the multiLane software interface, showing signal analysis for PCIe Gen4 16Gbps. The left screenshot shows a PRBS7 signal with jitter markers. The middle screenshot shows a signal transition with a red vertical line indicating a measurement point. The right screenshot shows an eye diagram with various measurement parameters listed in a table.

**Table 1: Measurements for ML-DSO-E (Eye Diagram)**

Measurements	Unit	Current	D
Peak To Peak	mV	871.33	X
Eye Amplitude	mV	739.72	X
Eye Height	mV	557.13	X
Eye Width	ps	56.64	X
Vertical Eye Closure (VEC by EH)	dB	2.46	X
Jitter rms	ps	1.06	X
Jitter P-P	ps	5.86	X
SNR		12.15	X
V rms	mV	338.26	X

**Table 2: Measurements for ML-DSO-J (Signal Transition)**

Measurements	Unit	Current	Delete
RJ rms	fs	538.64	X
V rms	mV	333.11	X

**Table 3: Measurements for ML-DSO-J (Signal Transition - Markers)**

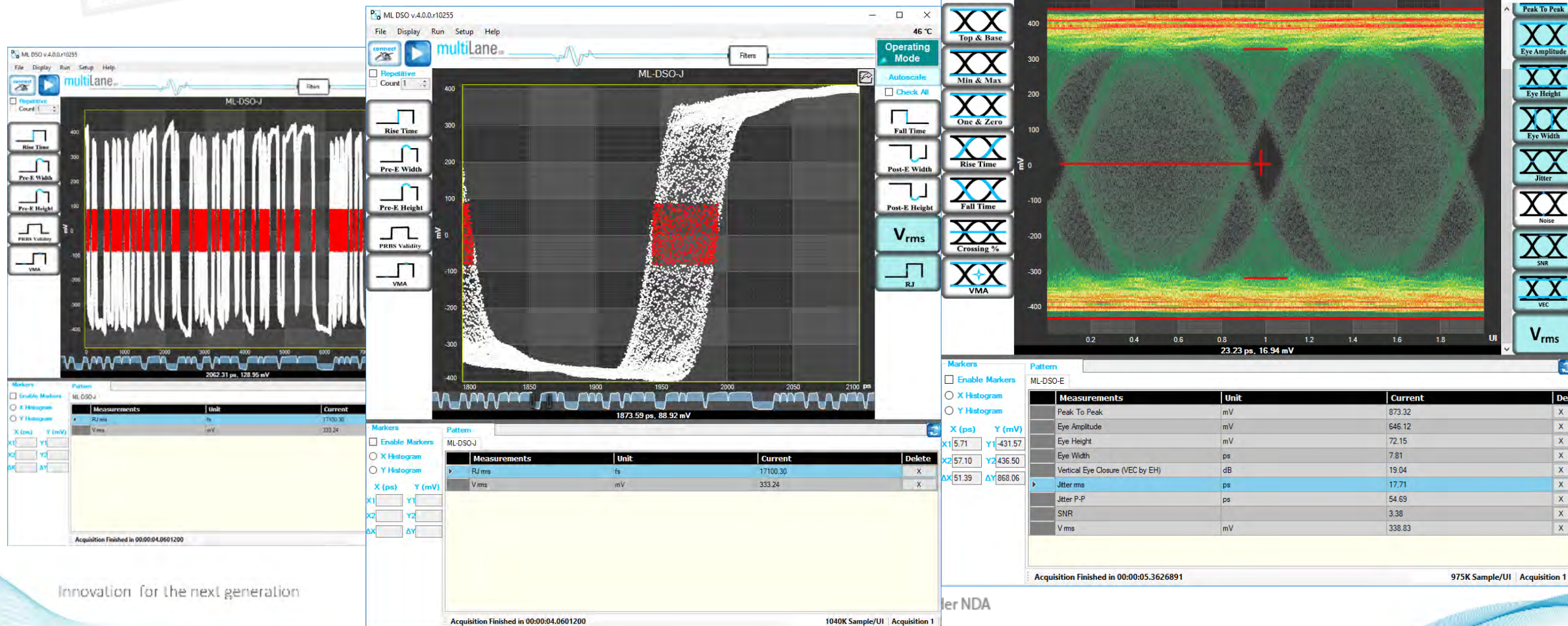
X (ps)	Y (mV)
X1: 5.71	Y1: -431.57
X2: 57.10	Y2: 436.50
ΔX: 51.39	ΔY: 868.06



# PCIe Gen4 16Gbps - Jitter Measurements

Jitter injected by software (50 ps)

PRBS7 – Signal generated with SJ Jitter insertion at ~2 MHz

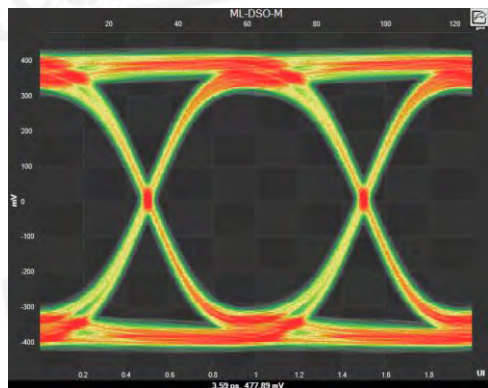




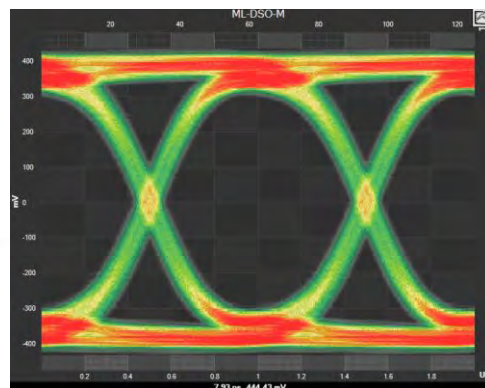
# PCIe Gen4 16Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~2 MHz

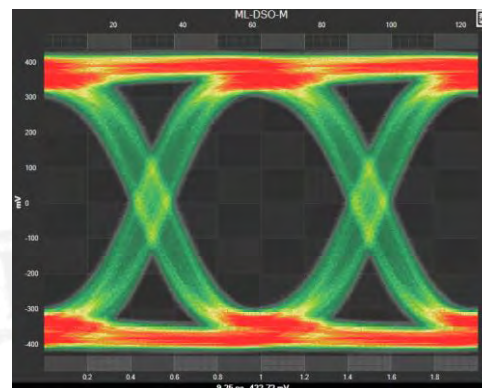
No Jitter



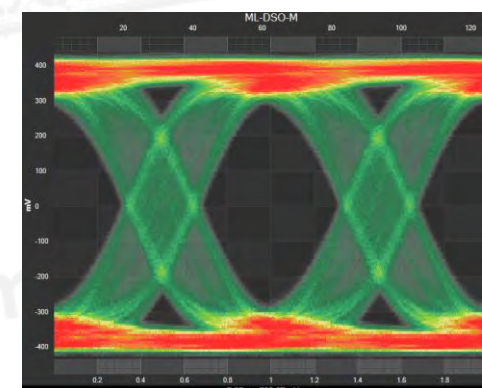
With SJ Jitter (5ps)



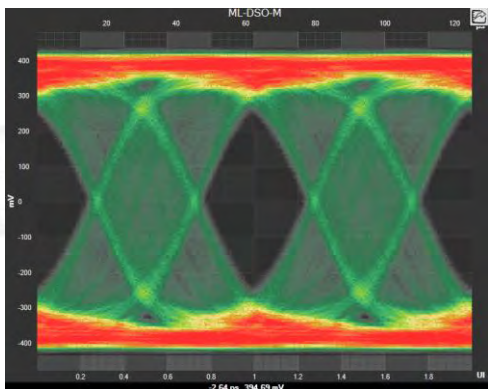
With SJ Jitter (10ps)



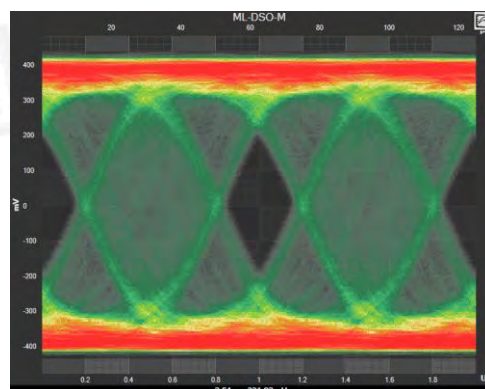
With SJ Jitter (20ps)



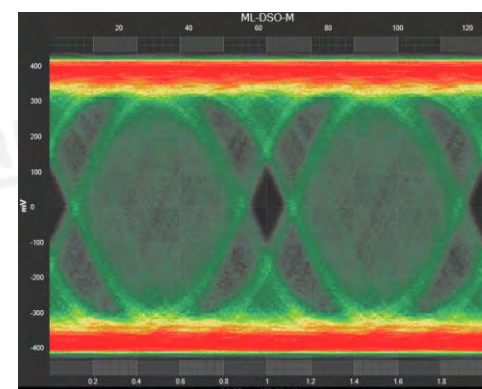
With SJ Jitter (30ps)



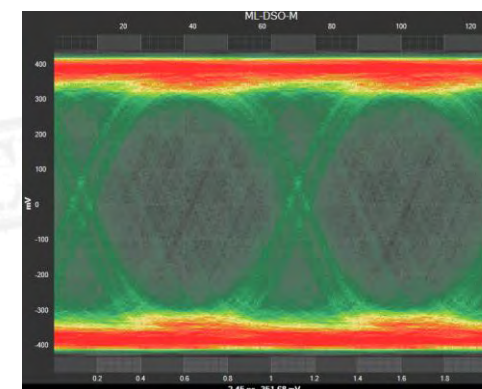
With SJ Jitter (40ps)



With SJ Jitter (50ps)



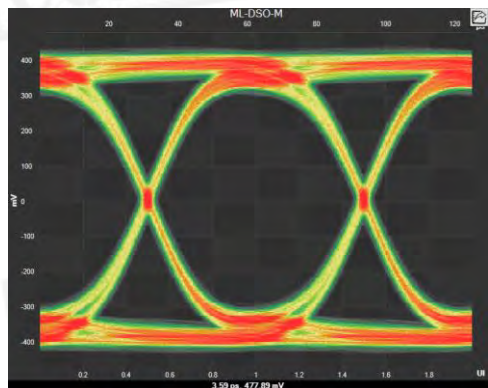
With SJ Jitter (60ps)



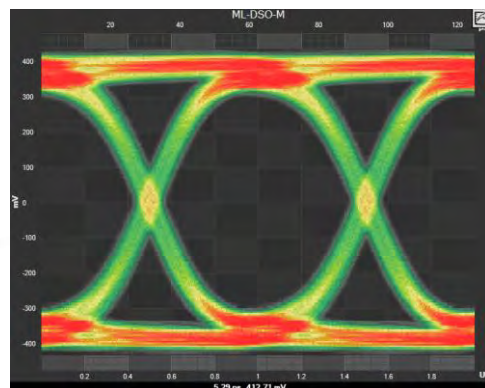
# PCIe Gen4 16Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~10 MHz

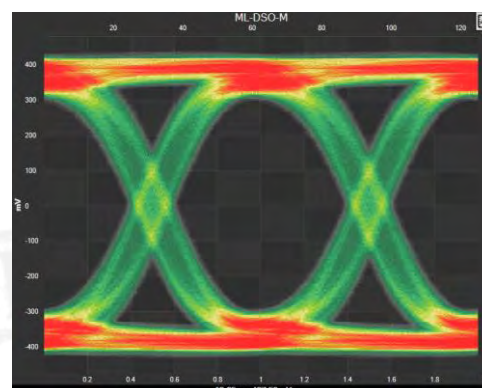
No Jitter



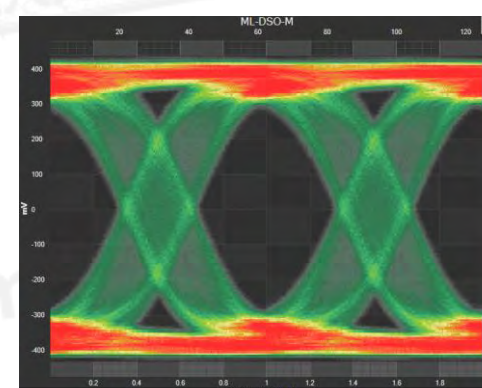
With SJ Jitter (5ps)



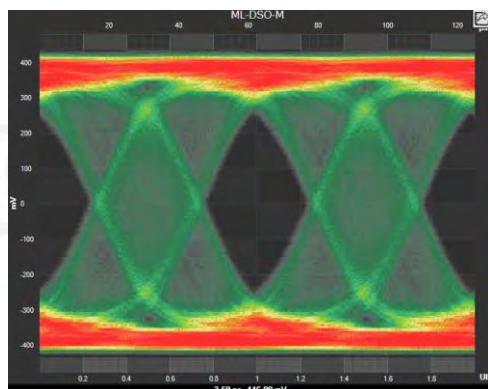
With SJ Jitter (10ps)



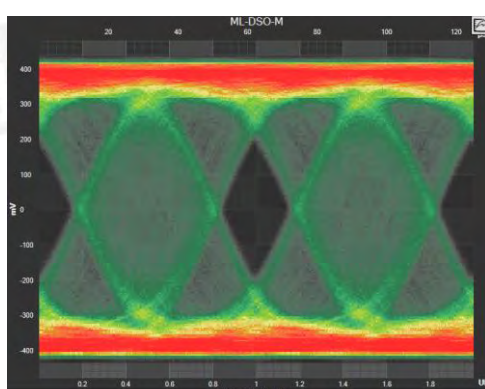
With SJ Jitter (20ps)



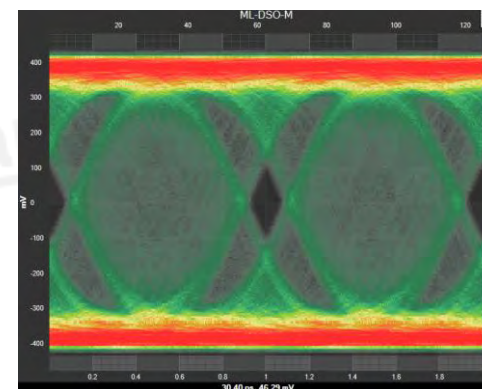
With SJ Jitter (30ps)



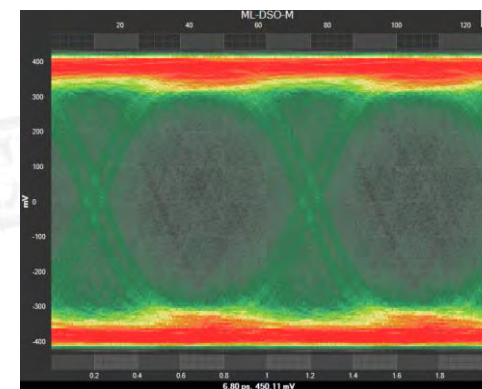
With SJ Jitter (40ps)



With SJ Jitter (50ps)



With SJ Jitter (60ps)

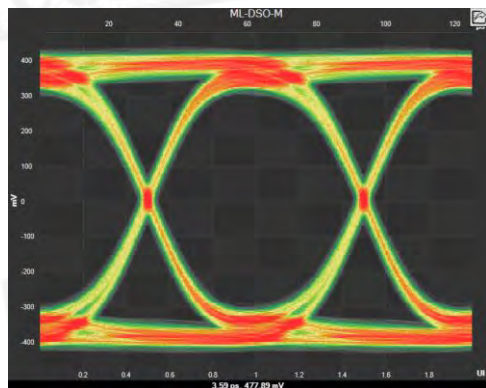




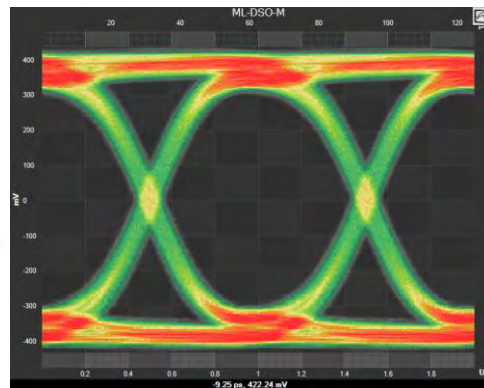
# PCIe Gen4 16Gbps - Jitter Measurements

PRBS11 – Signal generated with SJ Jitter insertion at ~100 MHz

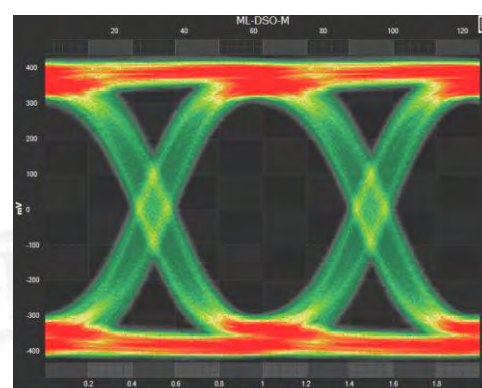
No Jitter



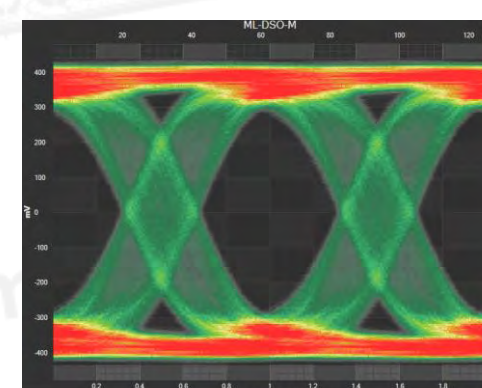
With SJ Jitter (5ps)



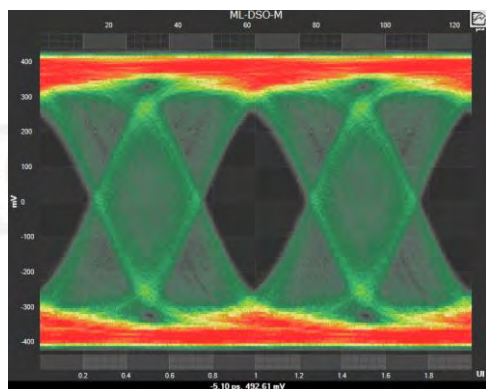
With SJ Jitter (10ps)



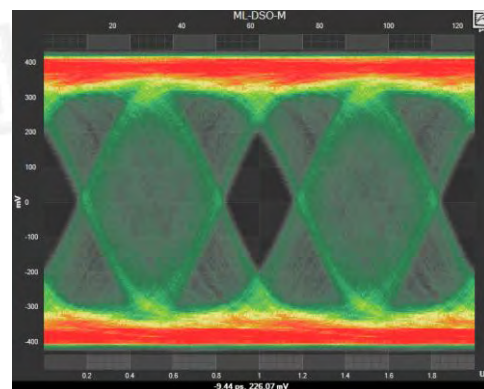
With SJ Jitter (20ps)



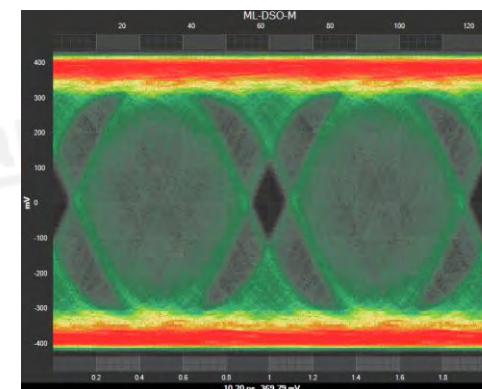
With SJ Jitter (30ps)



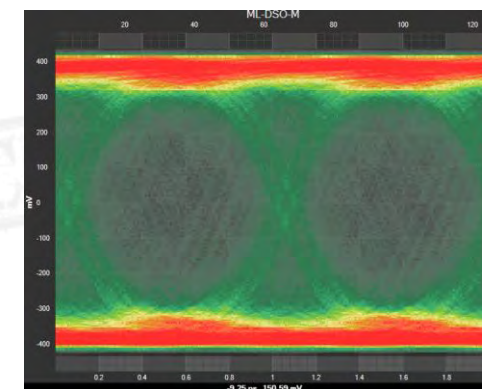
With SJ Jitter (40ps)



With SJ Jitter (50ps)

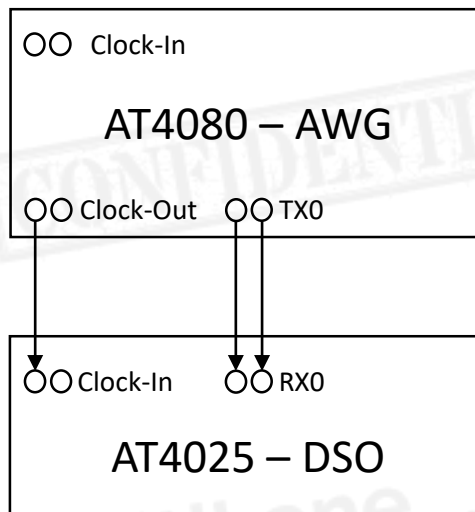


With SJ Jitter (60ps)



# Jitter Measurements – PRBS 11

ISI emulation and single tone Jitter injection by software for PCIe Gen 3

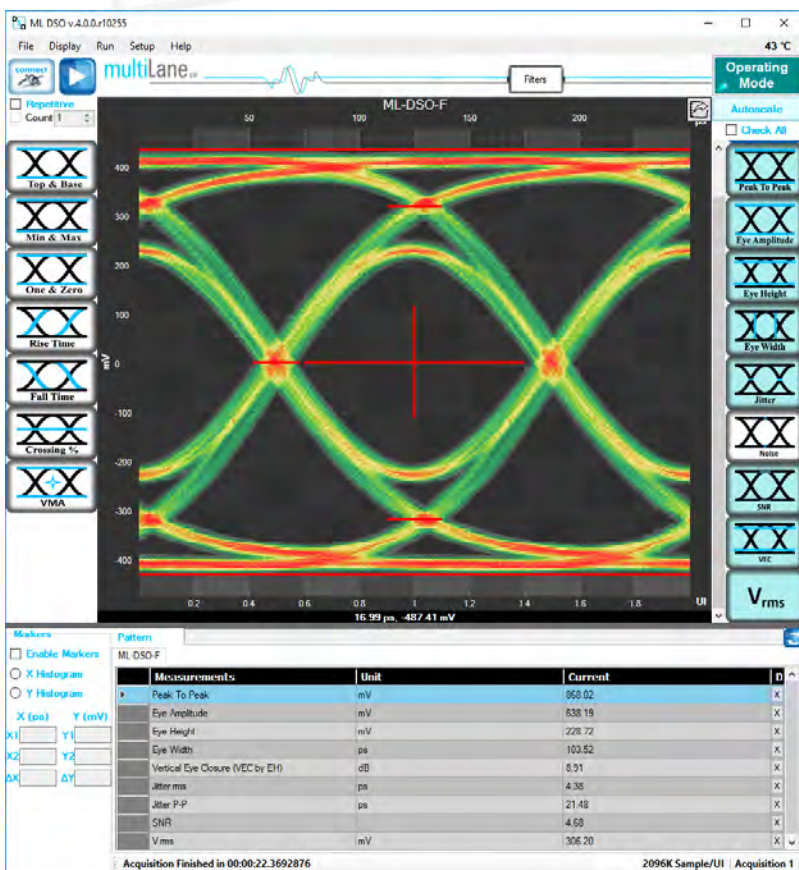




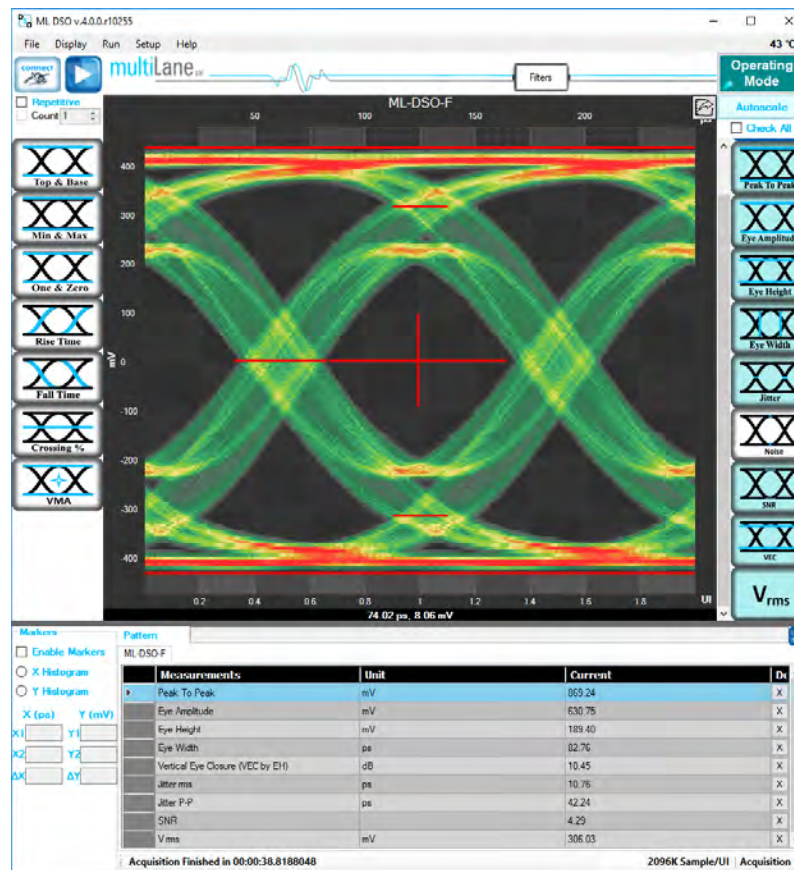
# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~2 MHz and ISI at **6dB**

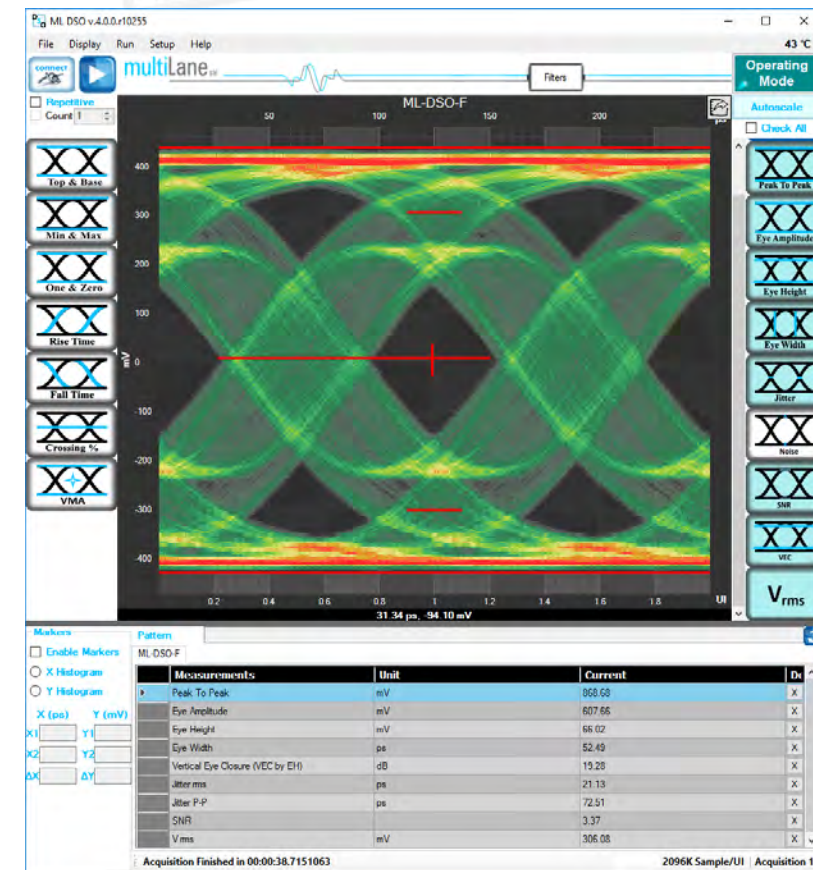
10 ps



30 ps



60 ps

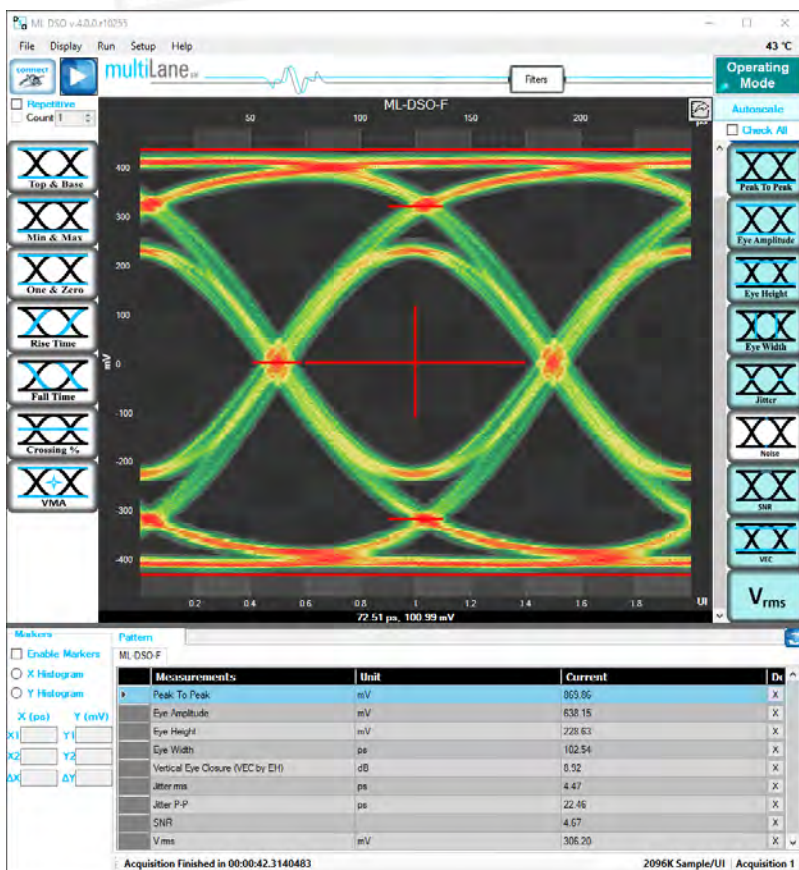




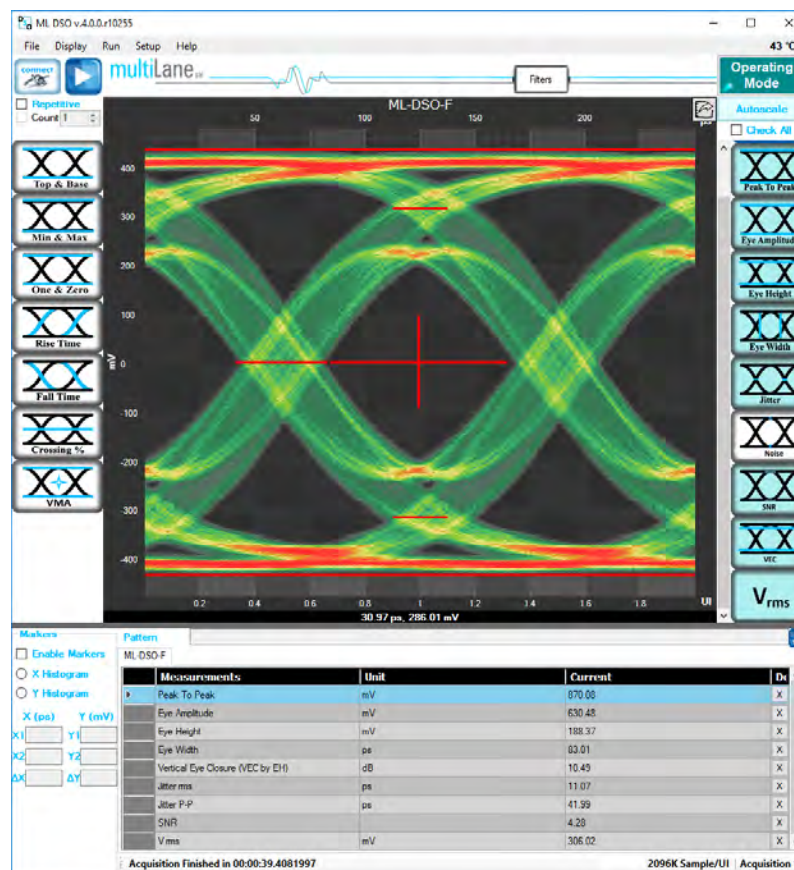
# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~10 MHz and ISI at **6dB**

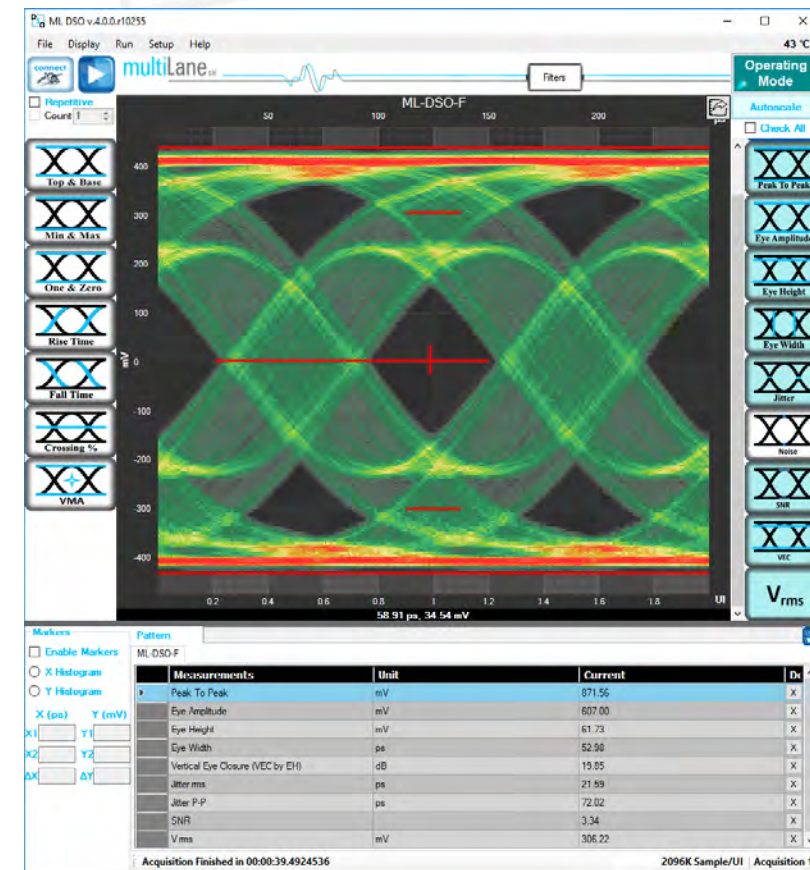
10 ps



30 ps



60 ps

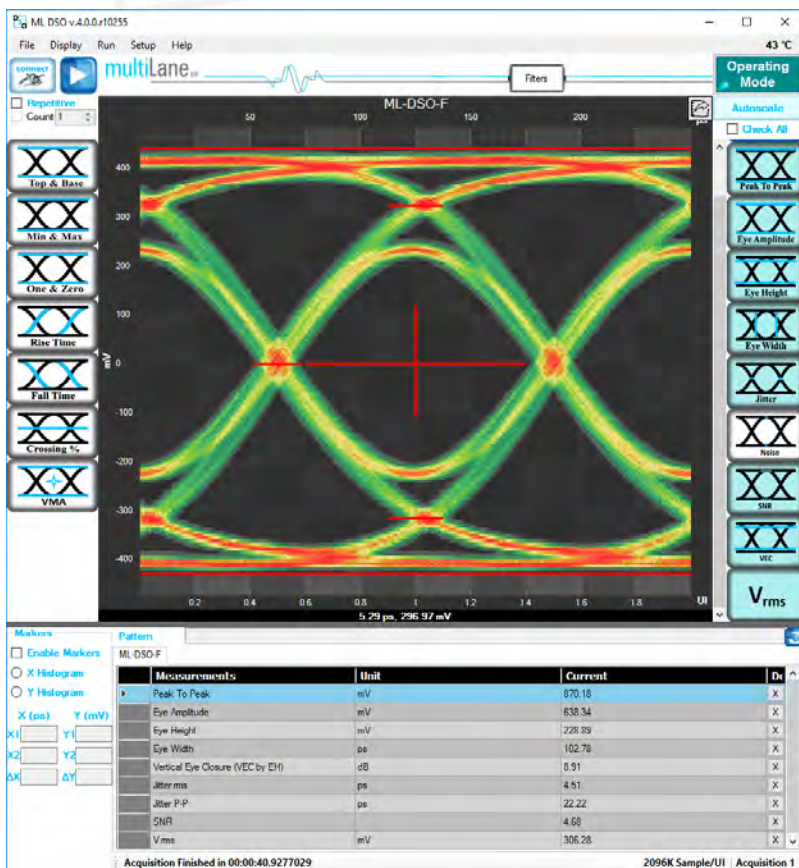




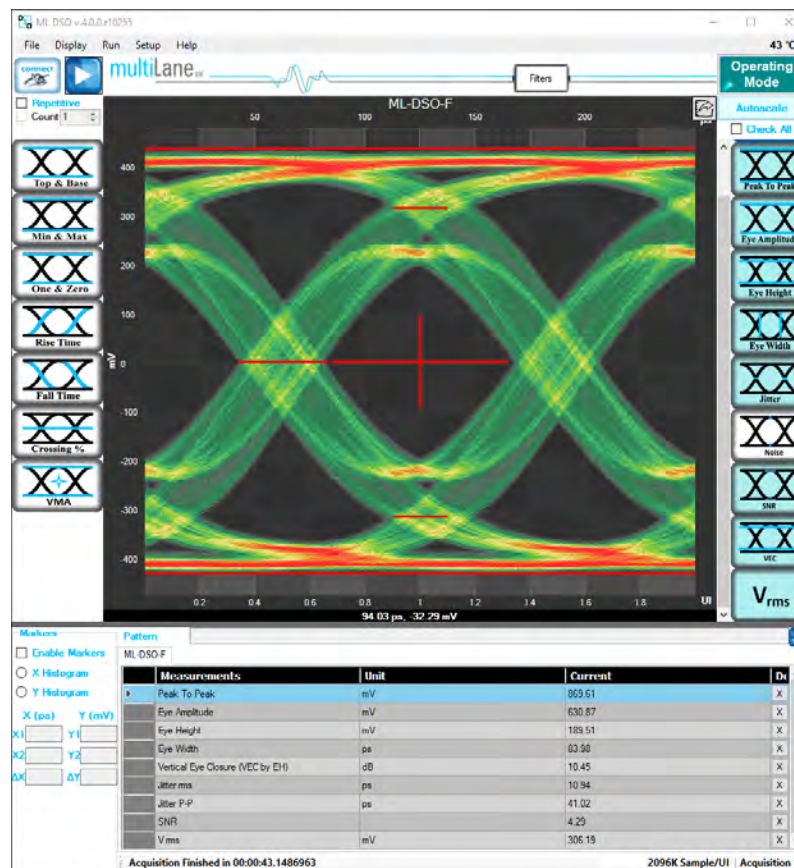
# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~100 MHz and ISI at **6dB**

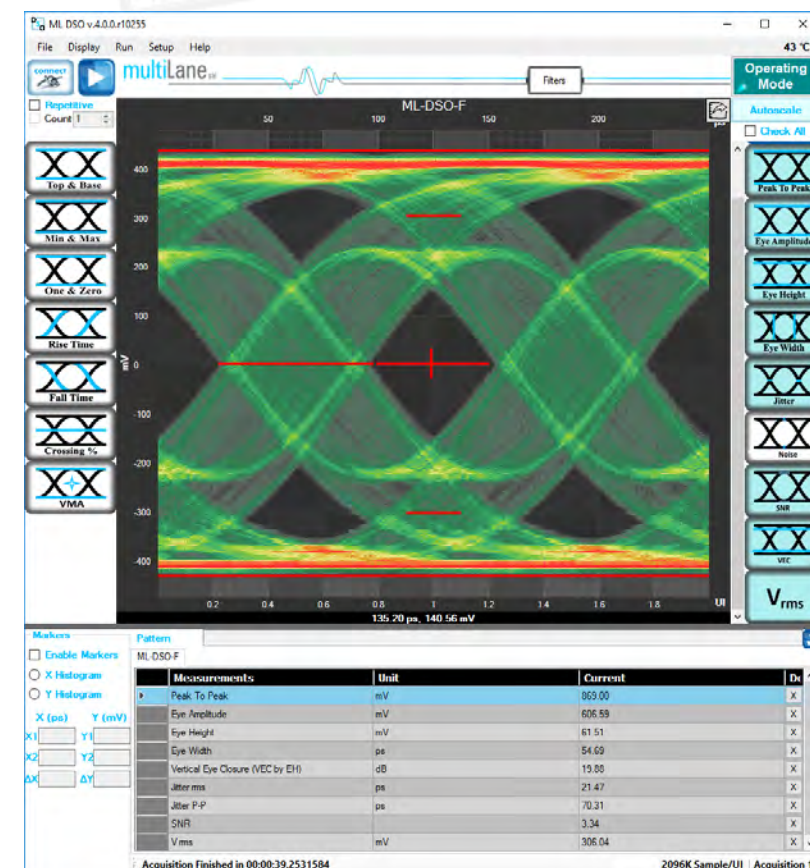
10 ps



30 ps



60 ps

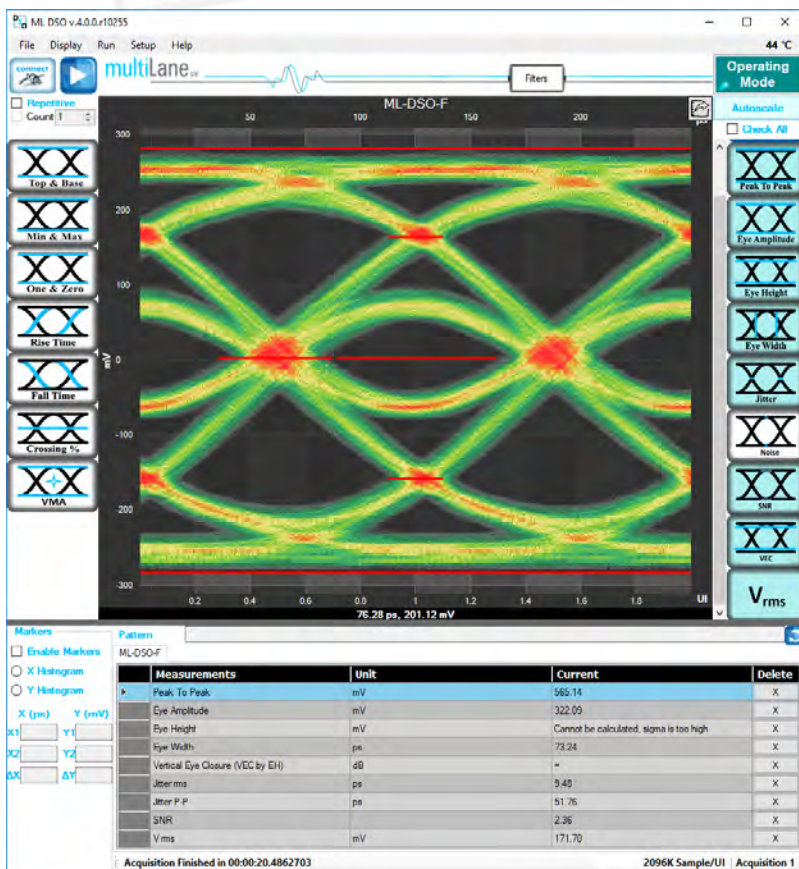




# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~2 MHz and ISI at **12dB**

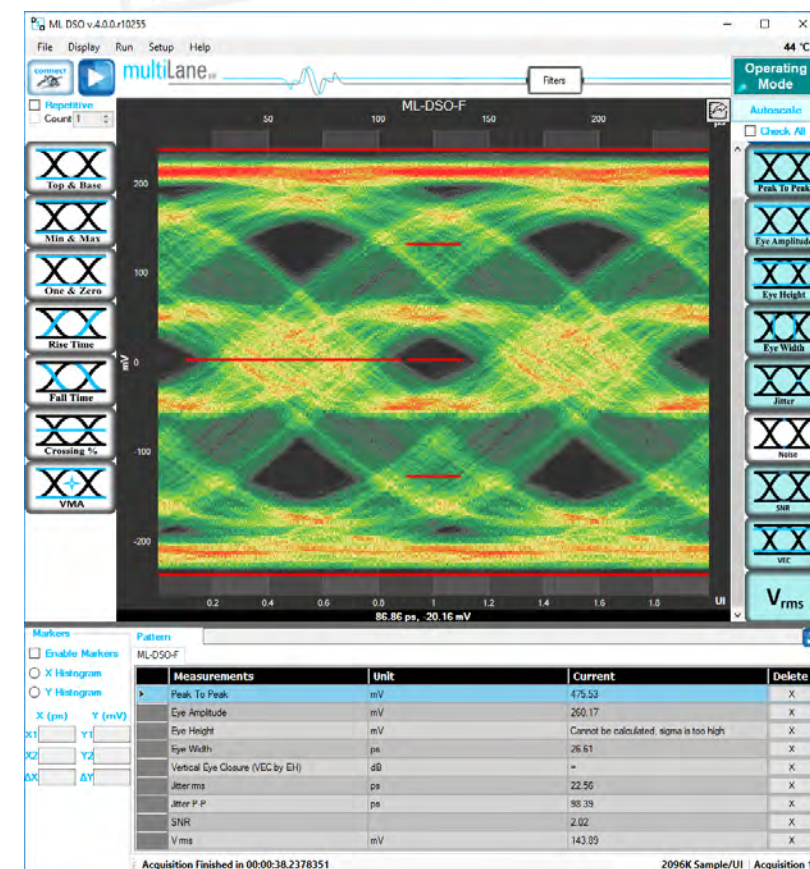
10 ps



30 ps



60 ps





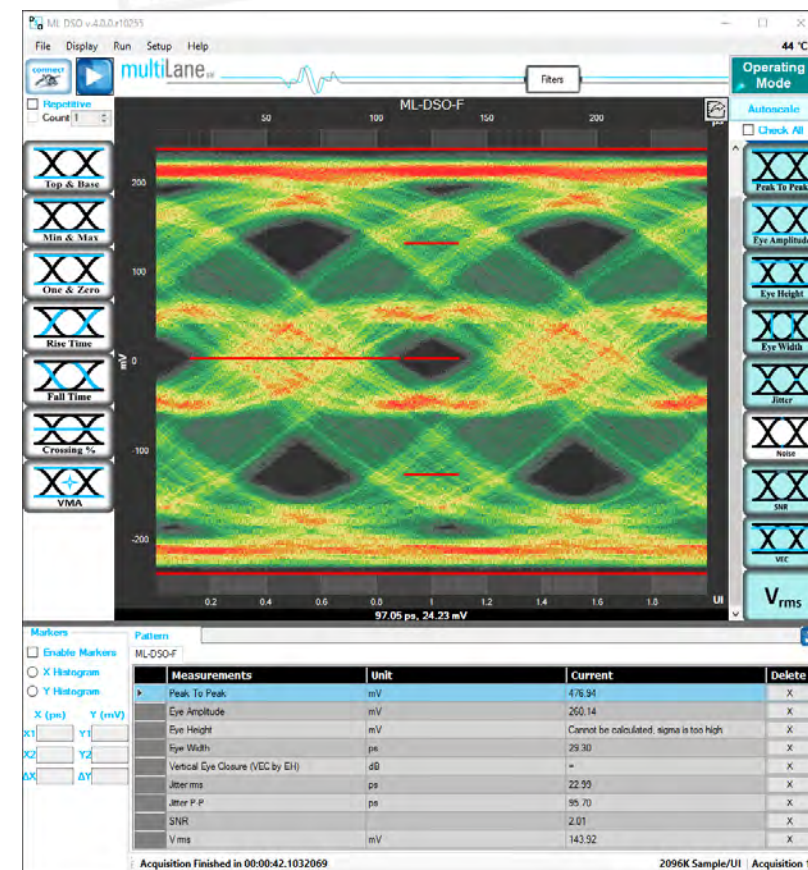
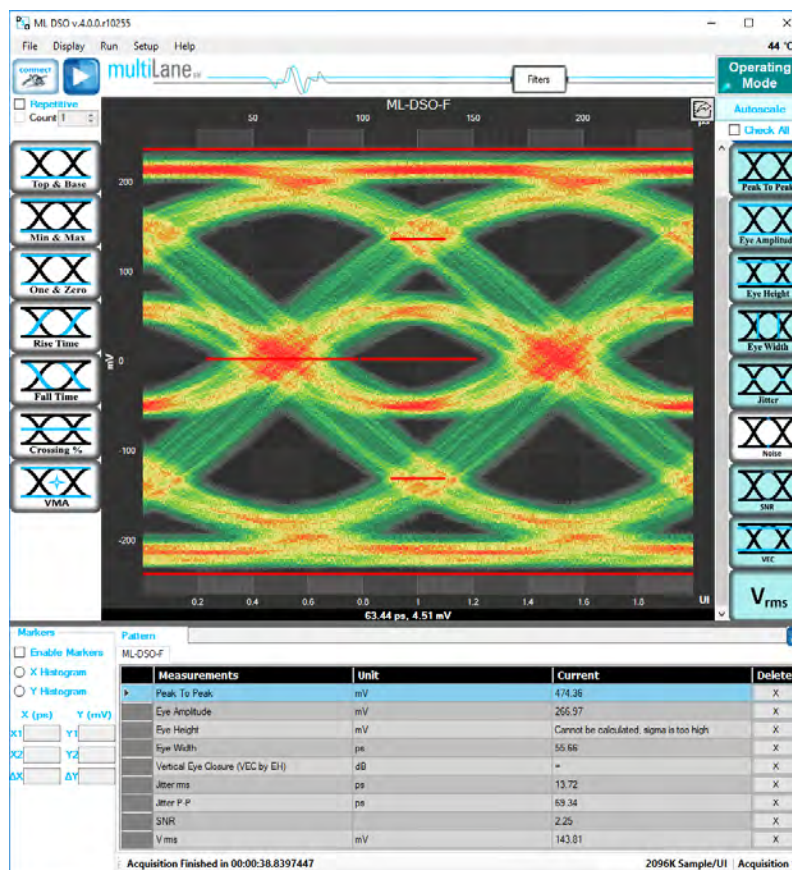
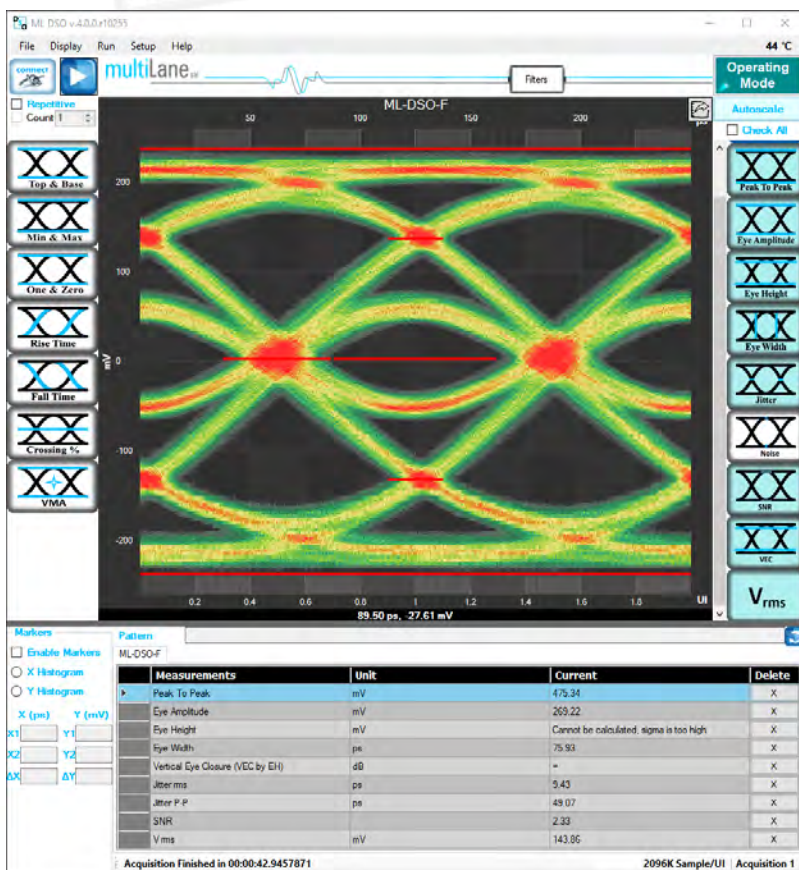
# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~10 MHz and ISI at **12dB**

10 ps

30 ps

60 ps

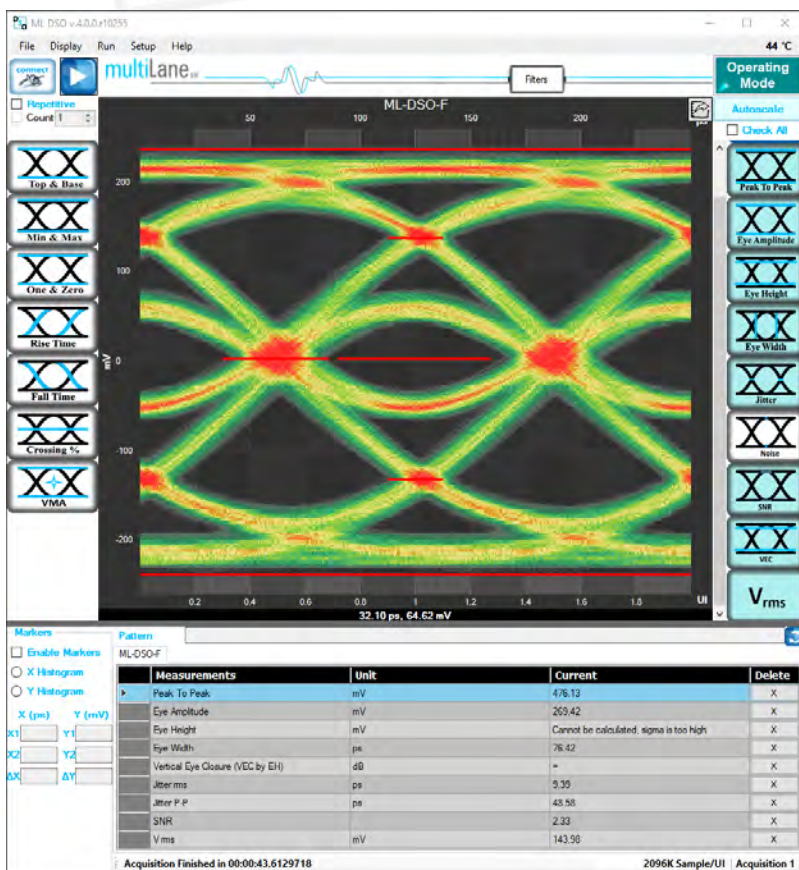




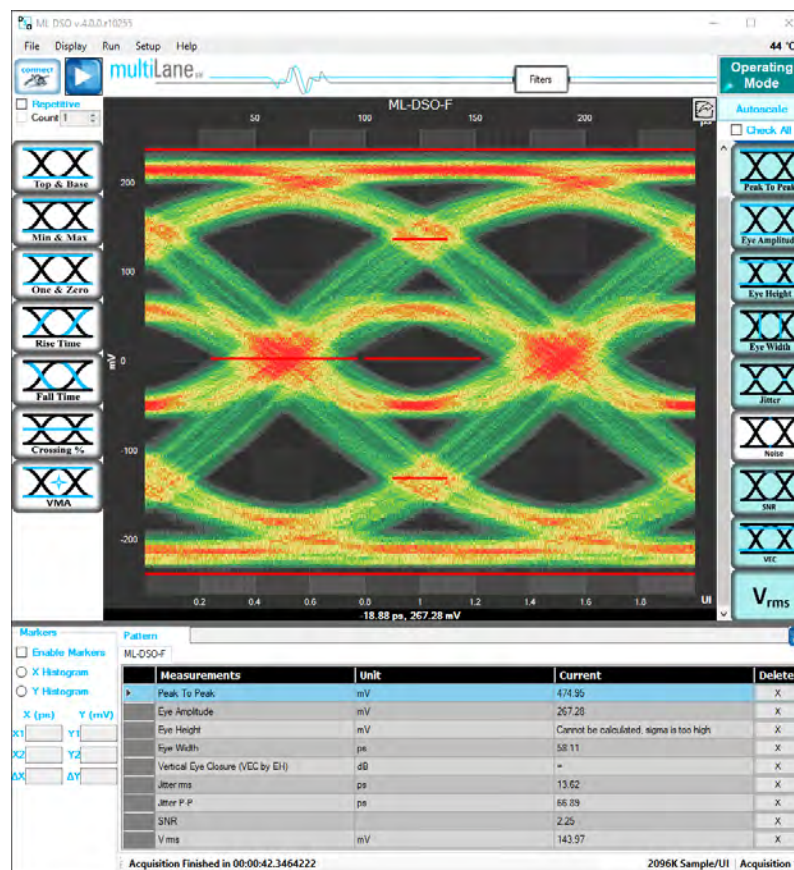
# PCIe Gen3 8Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – Signal generated with SJ Jitter insertion at ~100 MHz and ISI at **12dB**

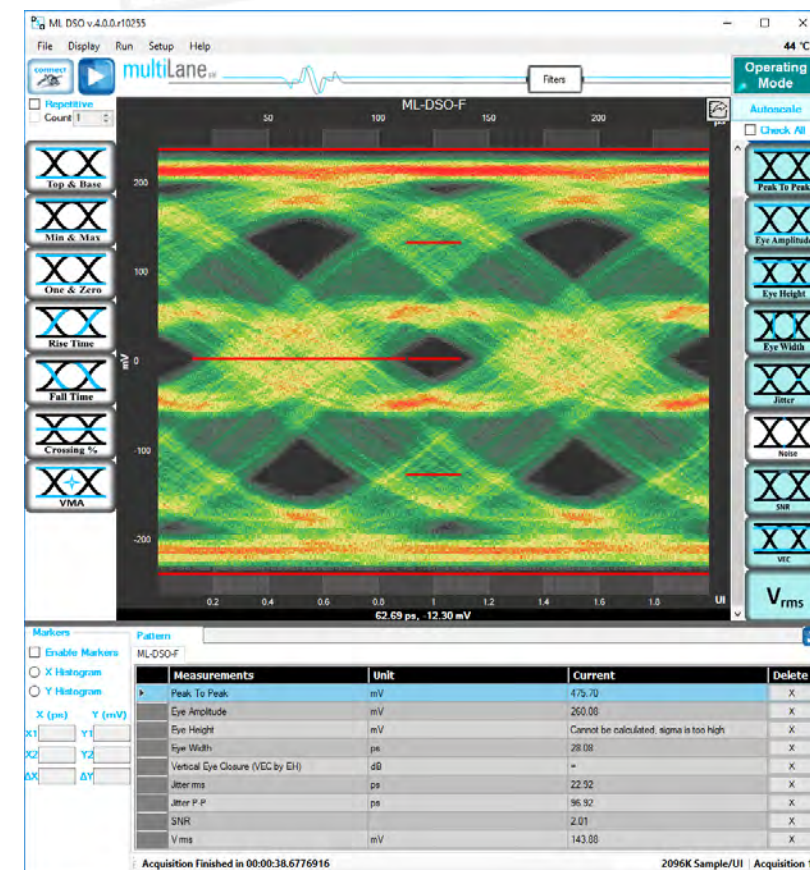
10 ps



30 ps



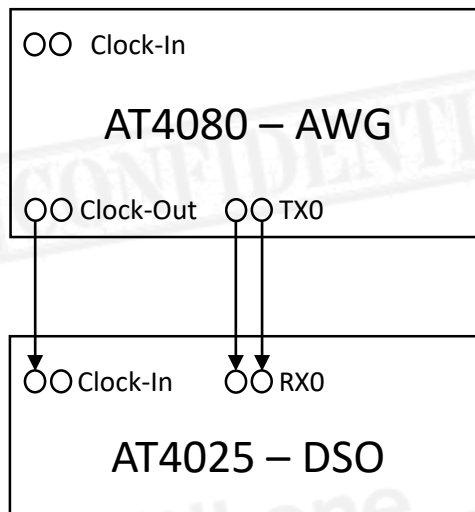
60 ps





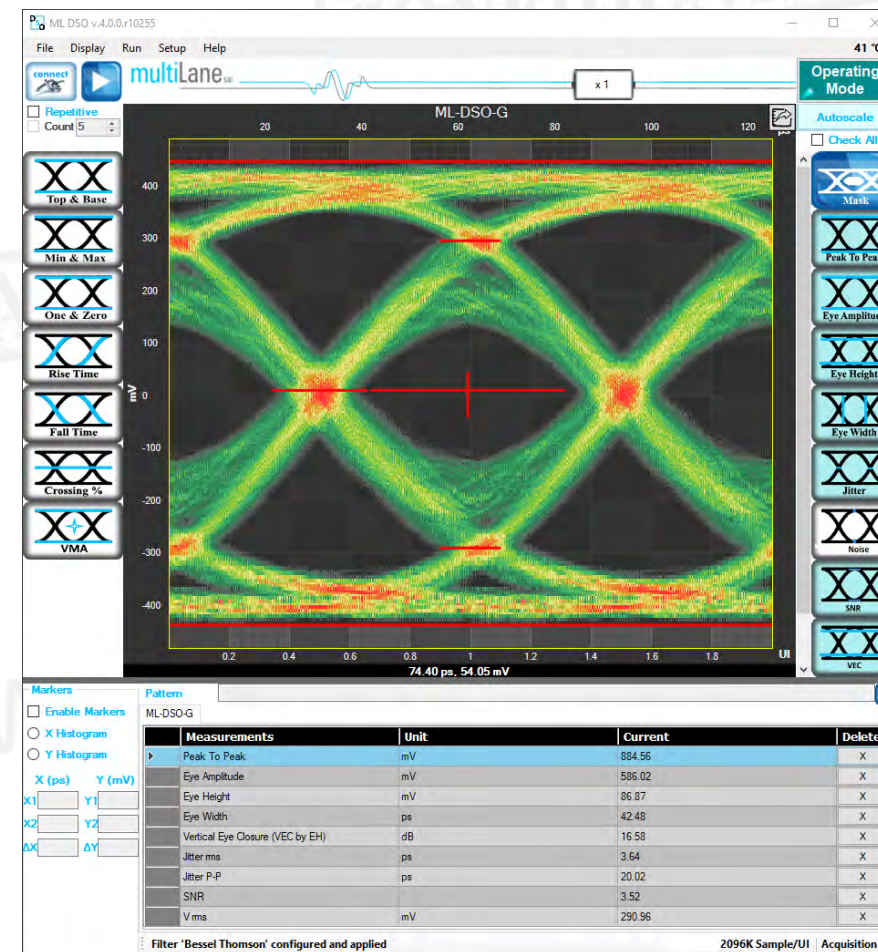
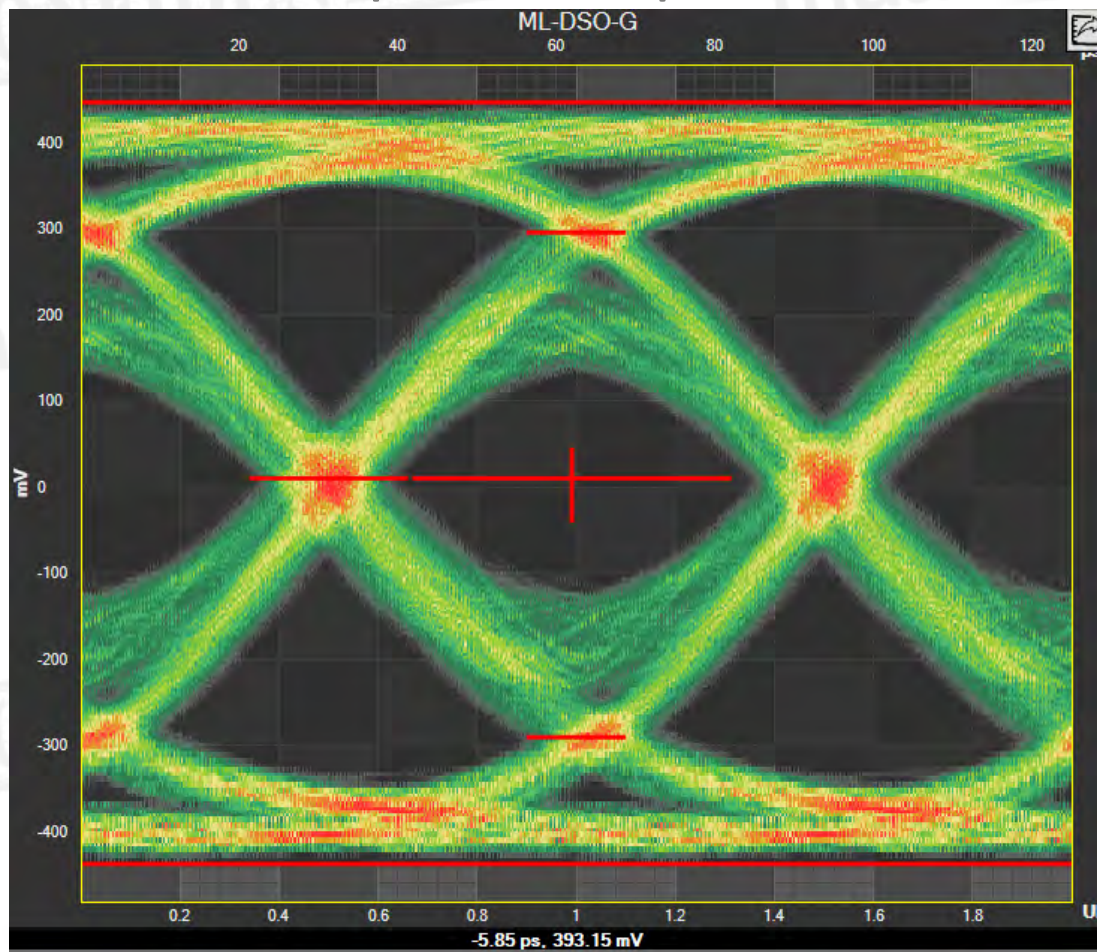
# Jitter Measurements – PRBS 11

Dual tones Jitter injection by software for PCIe Gen 4



# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

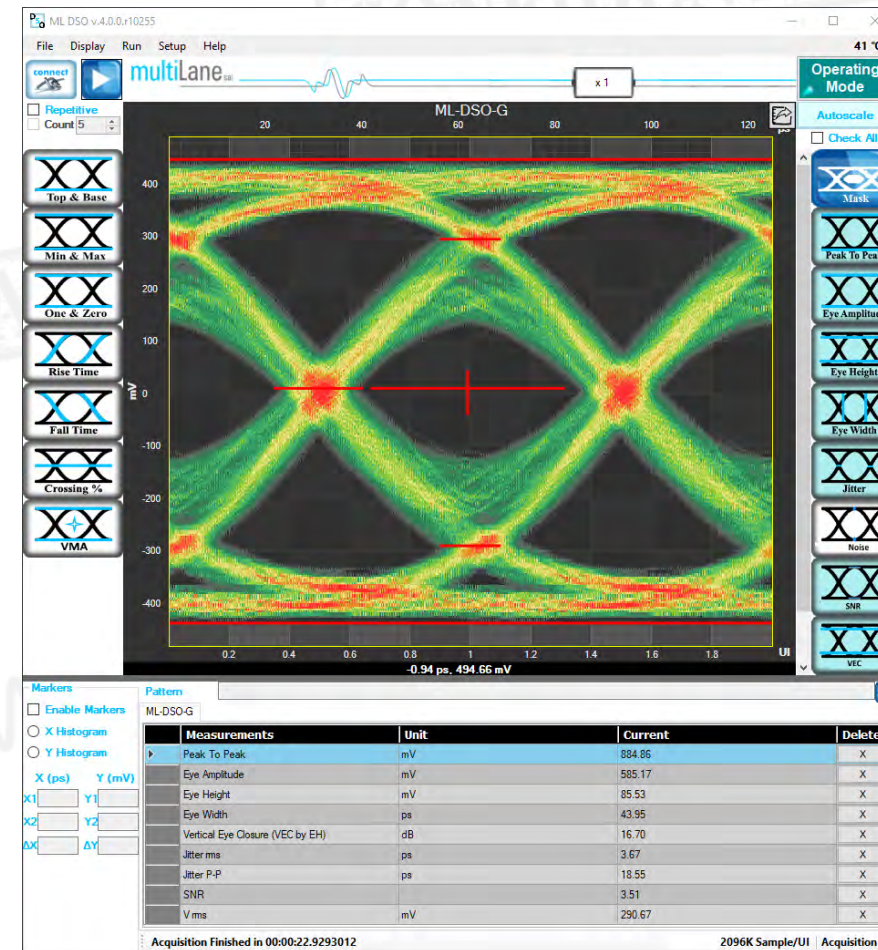
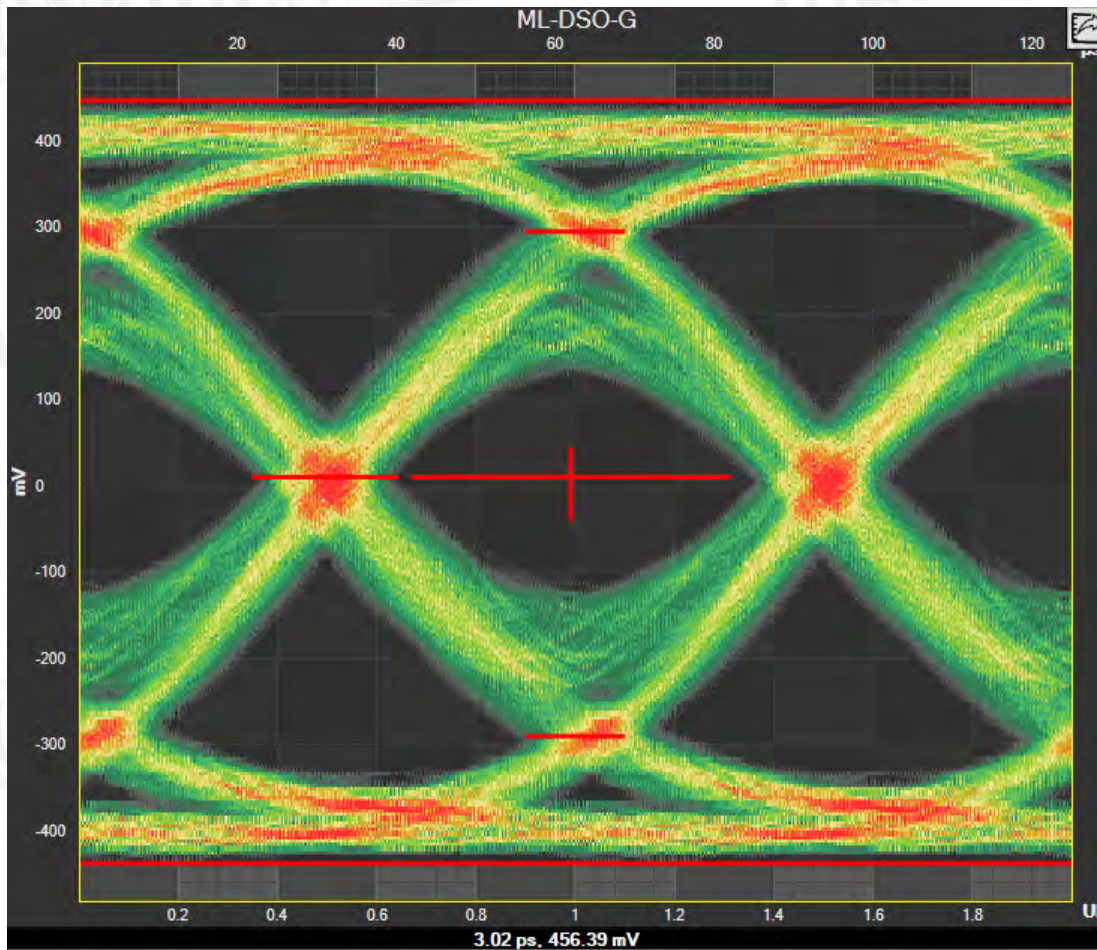
PRBS11 – SJ Amplitude 2 ps at **~60 MHz** and **~1 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

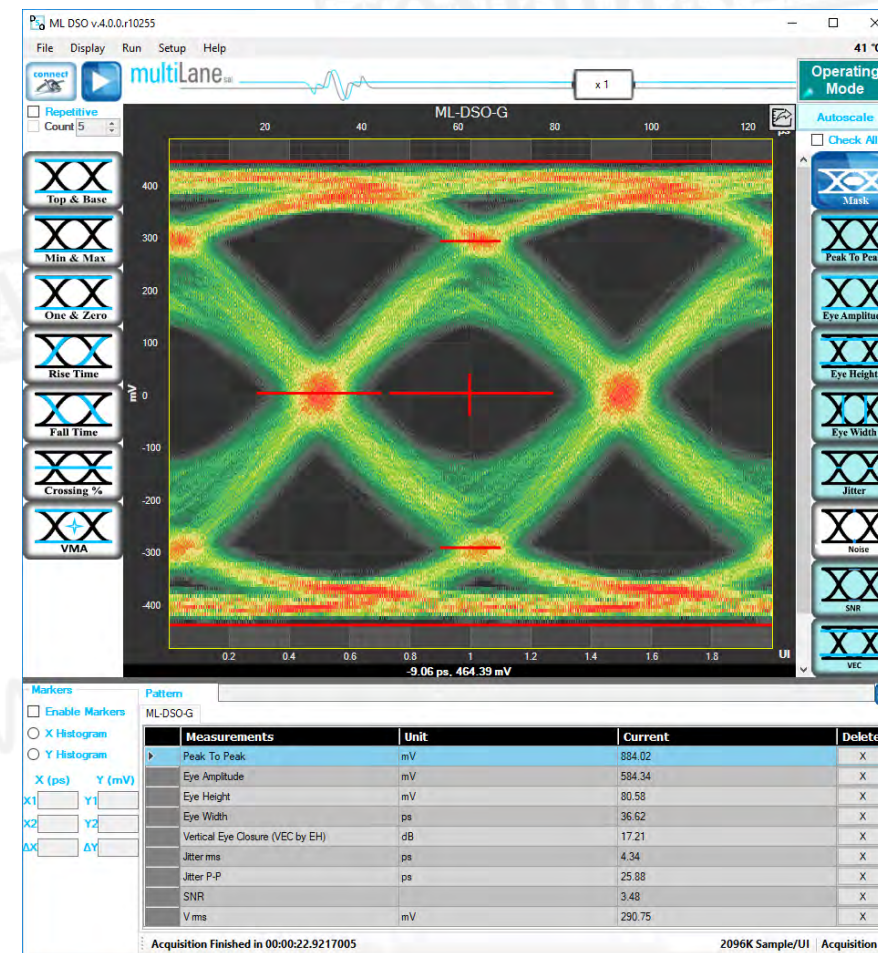
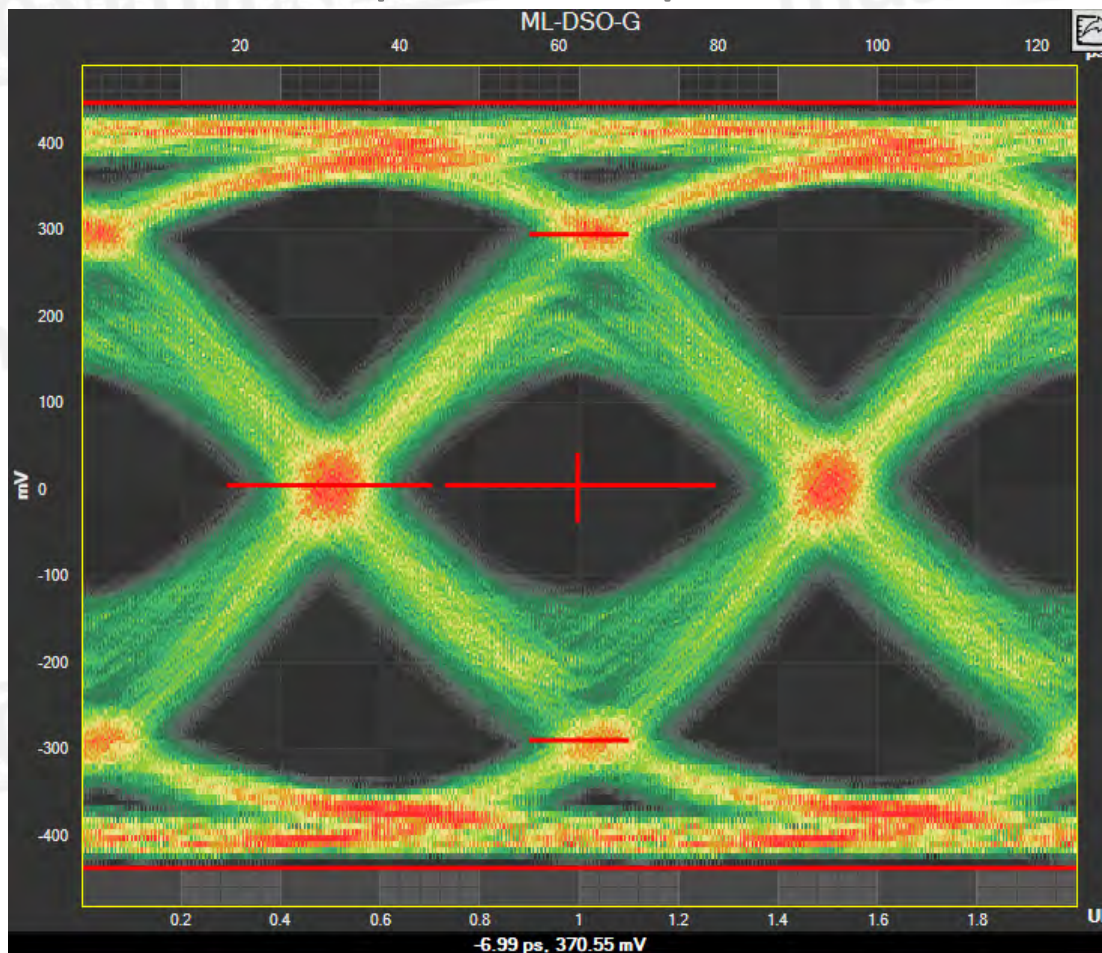
PRBS11 – SJ Amplitude 2 ps at **~60 MHz** and **~4 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

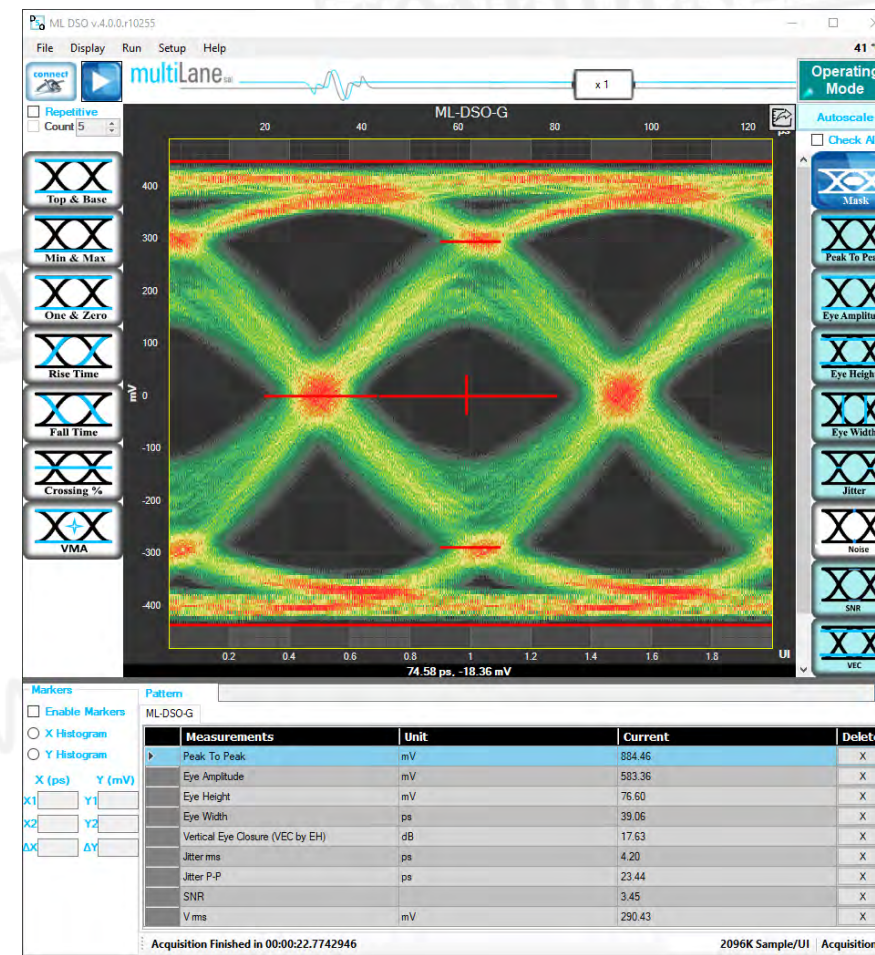
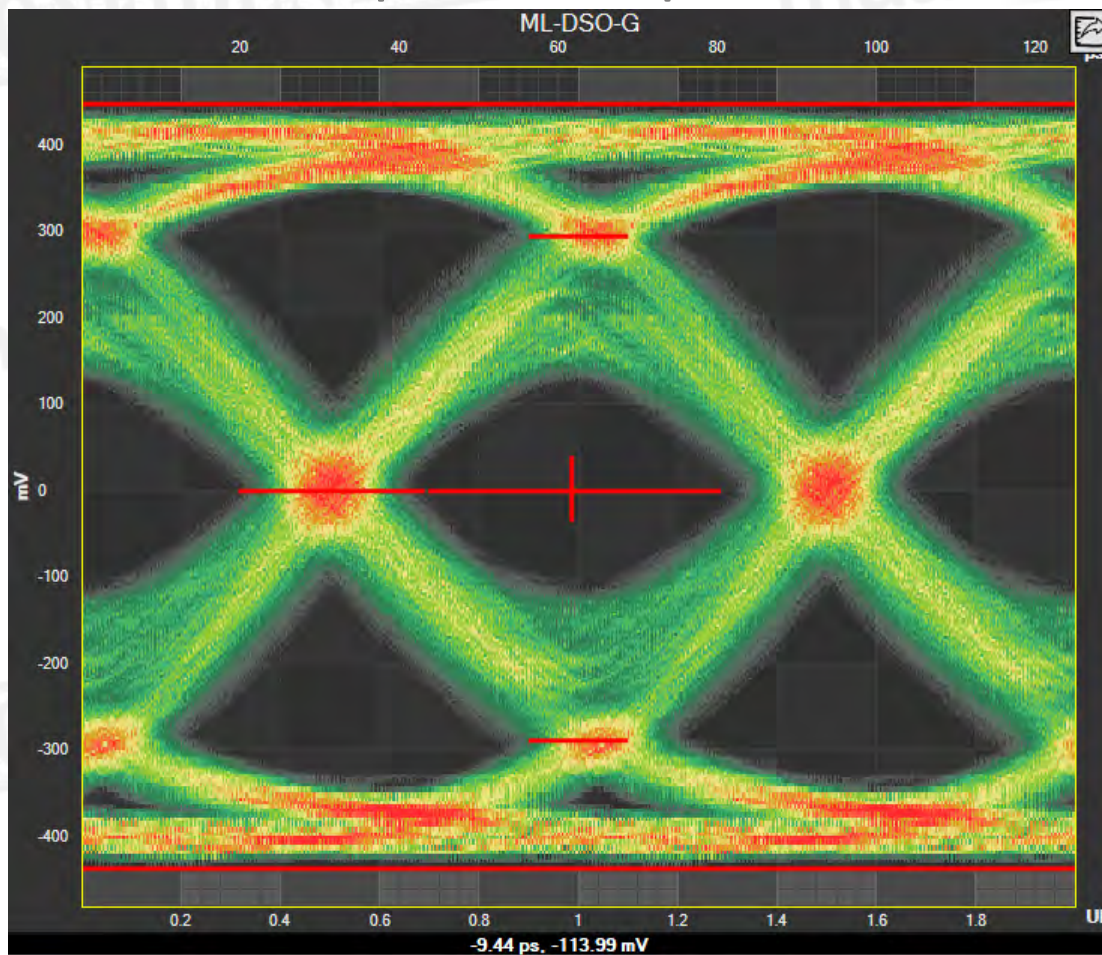
PRBS11 – SJ Amplitude 5 ps at **~60 MHz** and **~1 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

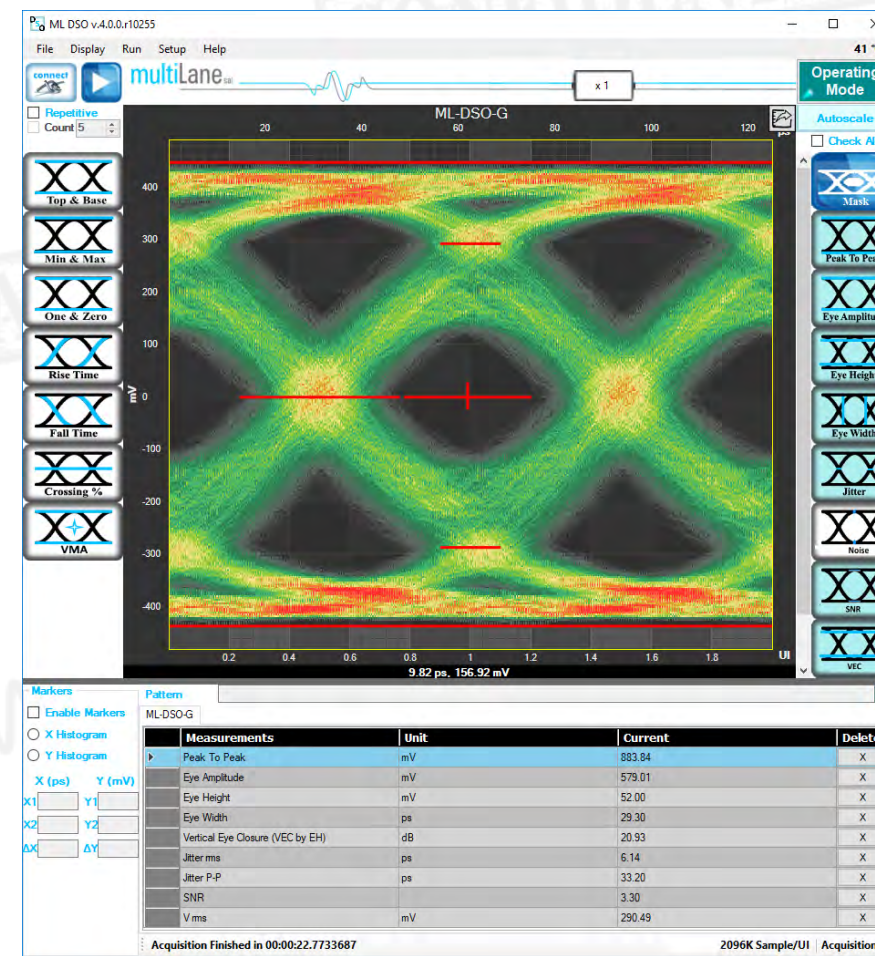
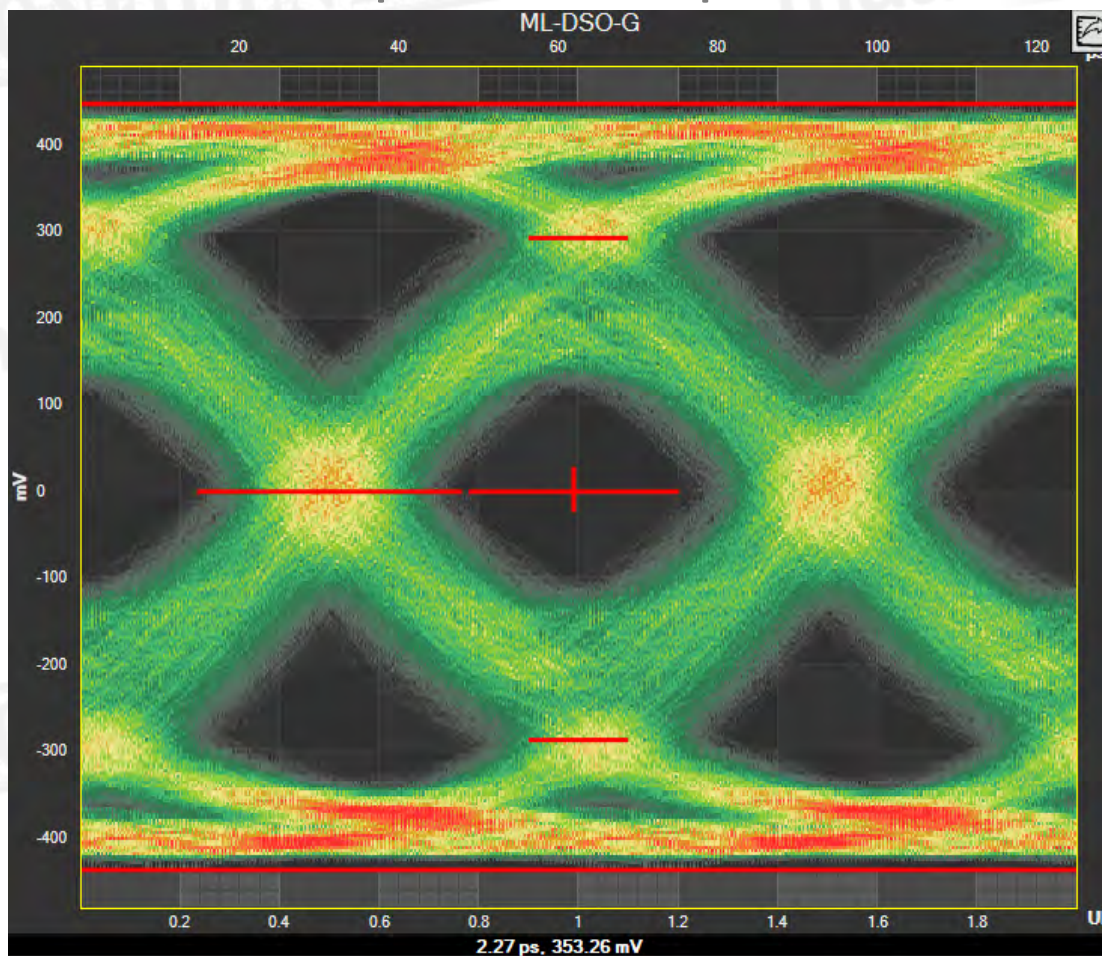
PRBS11 – SJ Amplitude 5 ps at **~60 MHz** and **~4 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

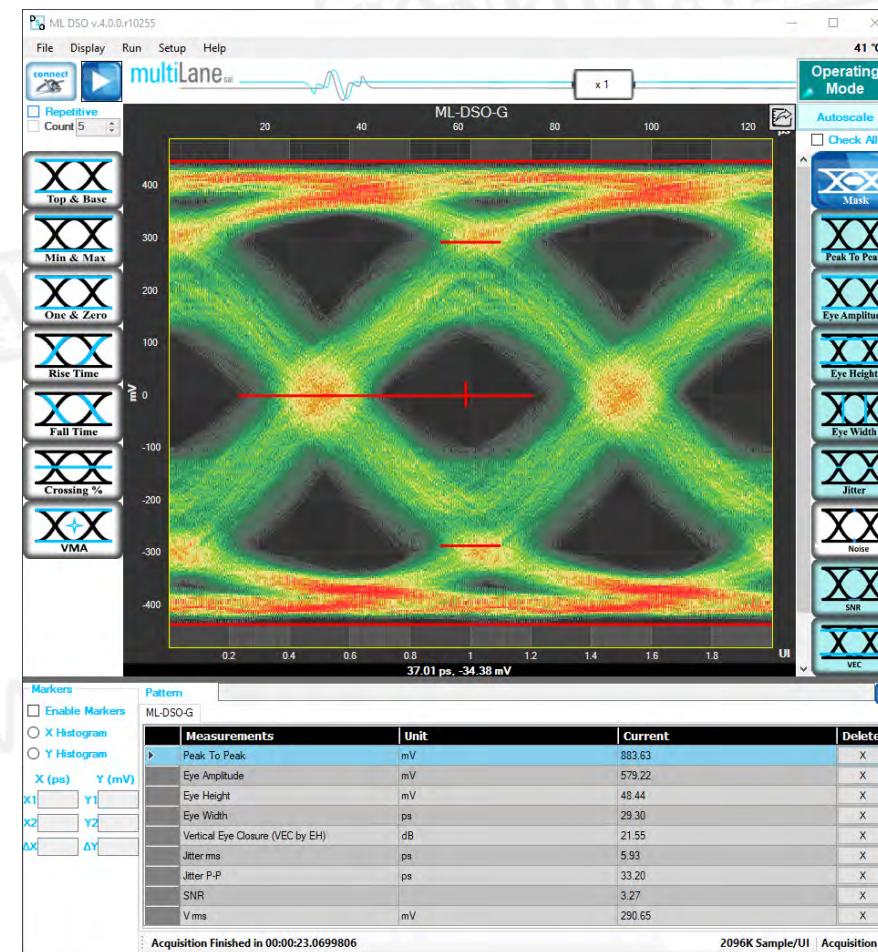
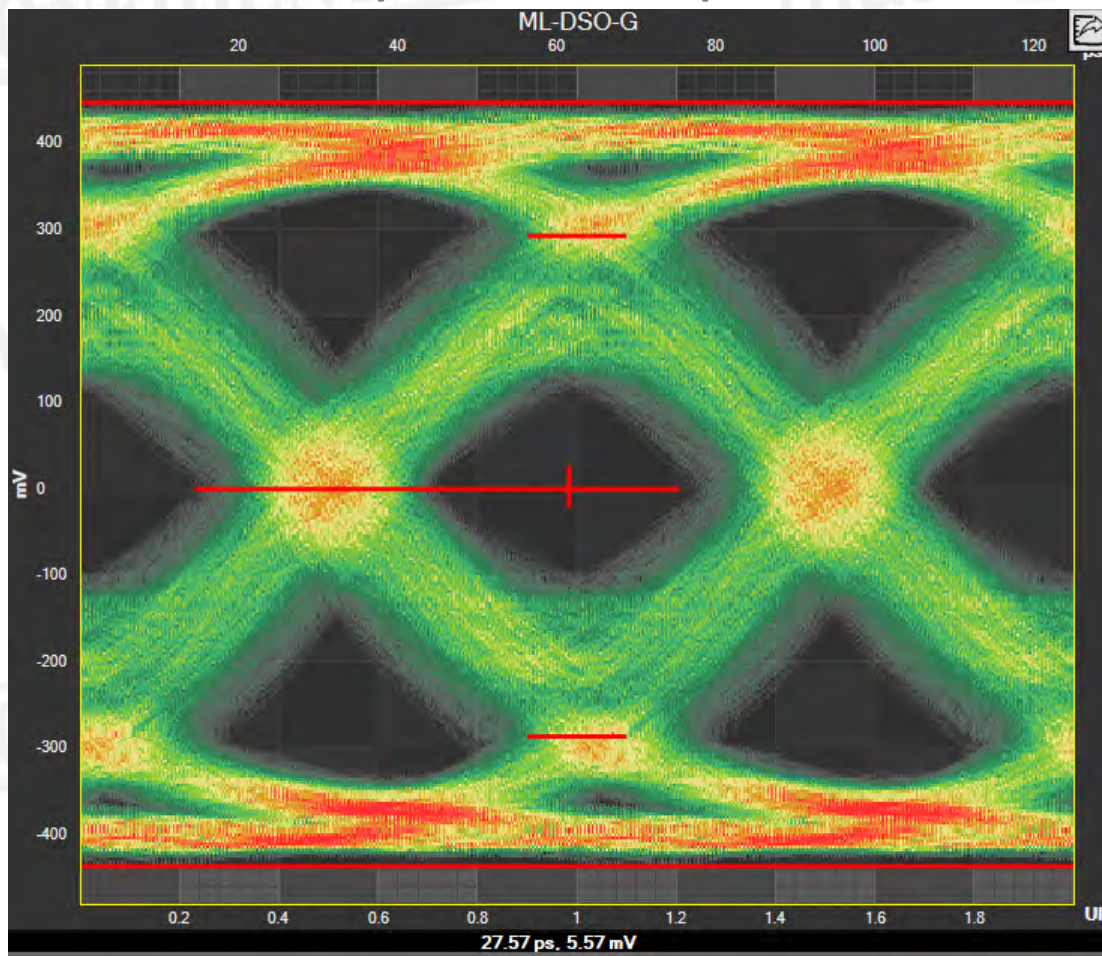
PRBS11 – SJ Amplitude 10 ps at **~60 MHz** and **~1 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

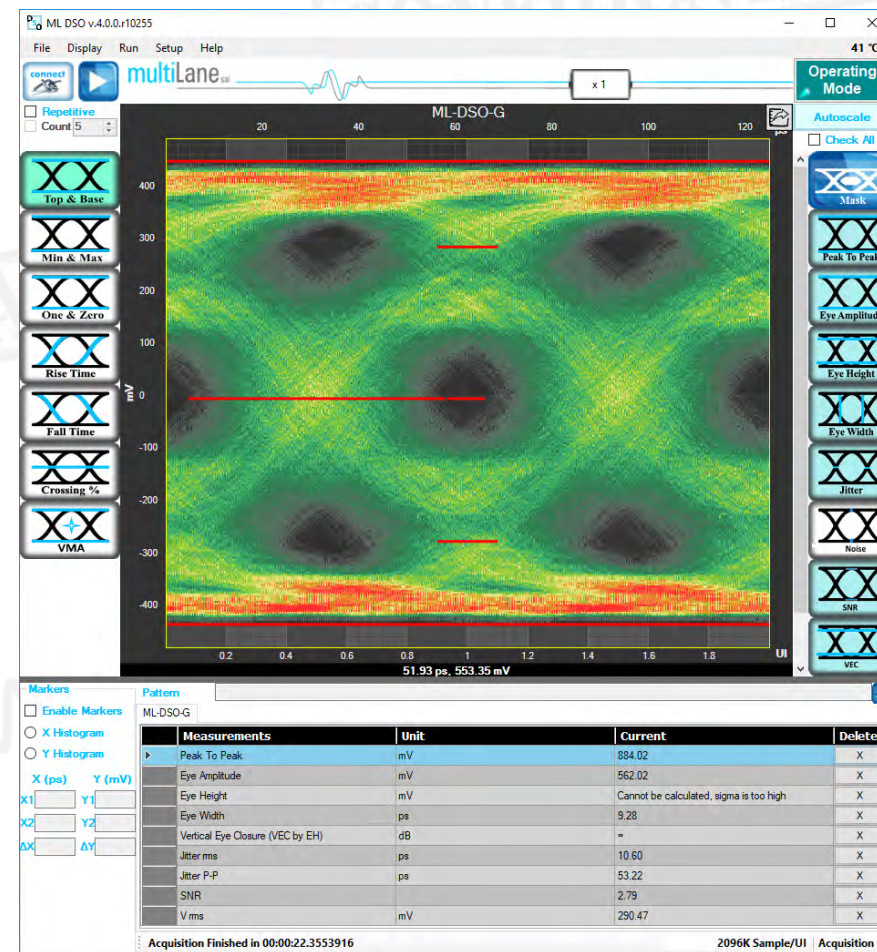
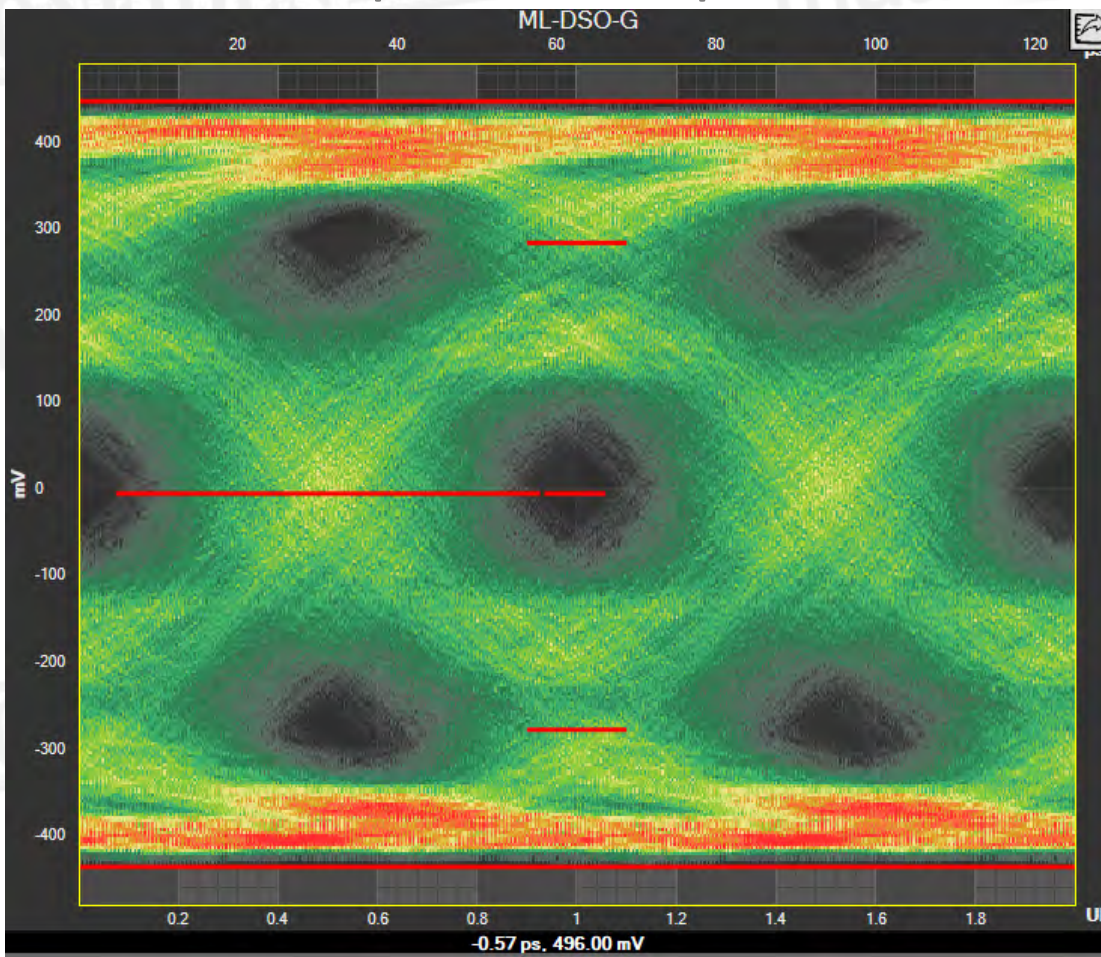
PRBS11 – SJ Amplitude 10 ps at **~60 MHz** and **~4 MHz** with ISI at **6dB**





# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

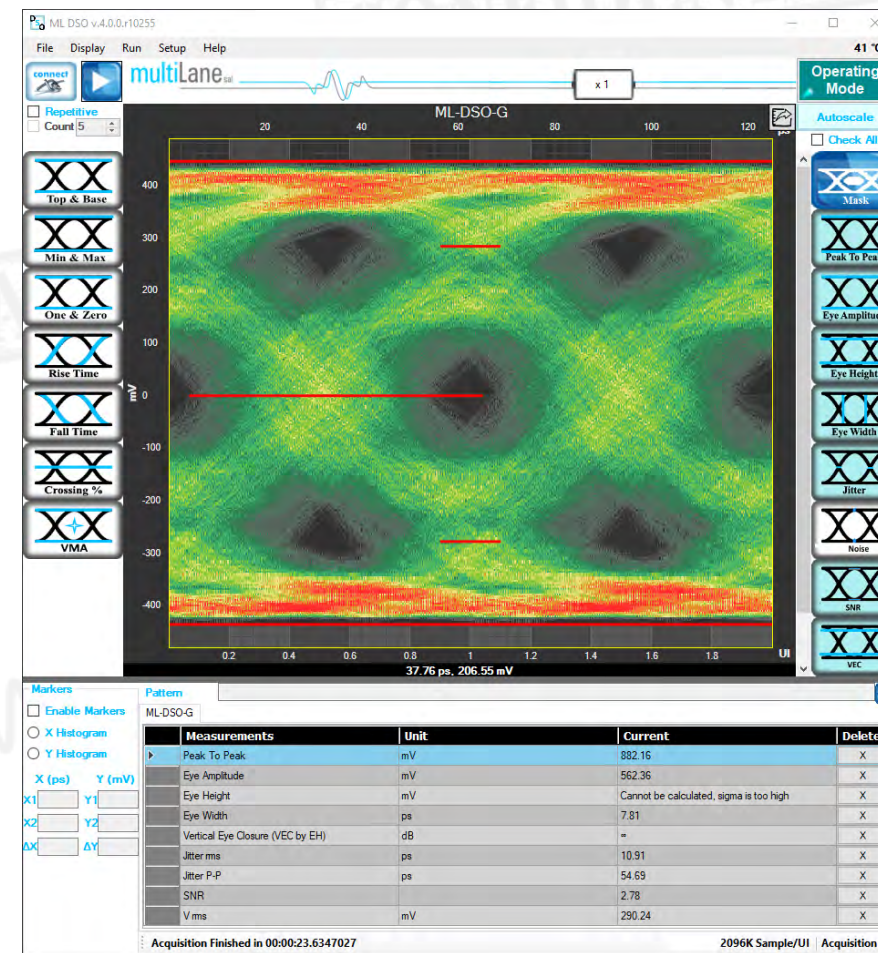
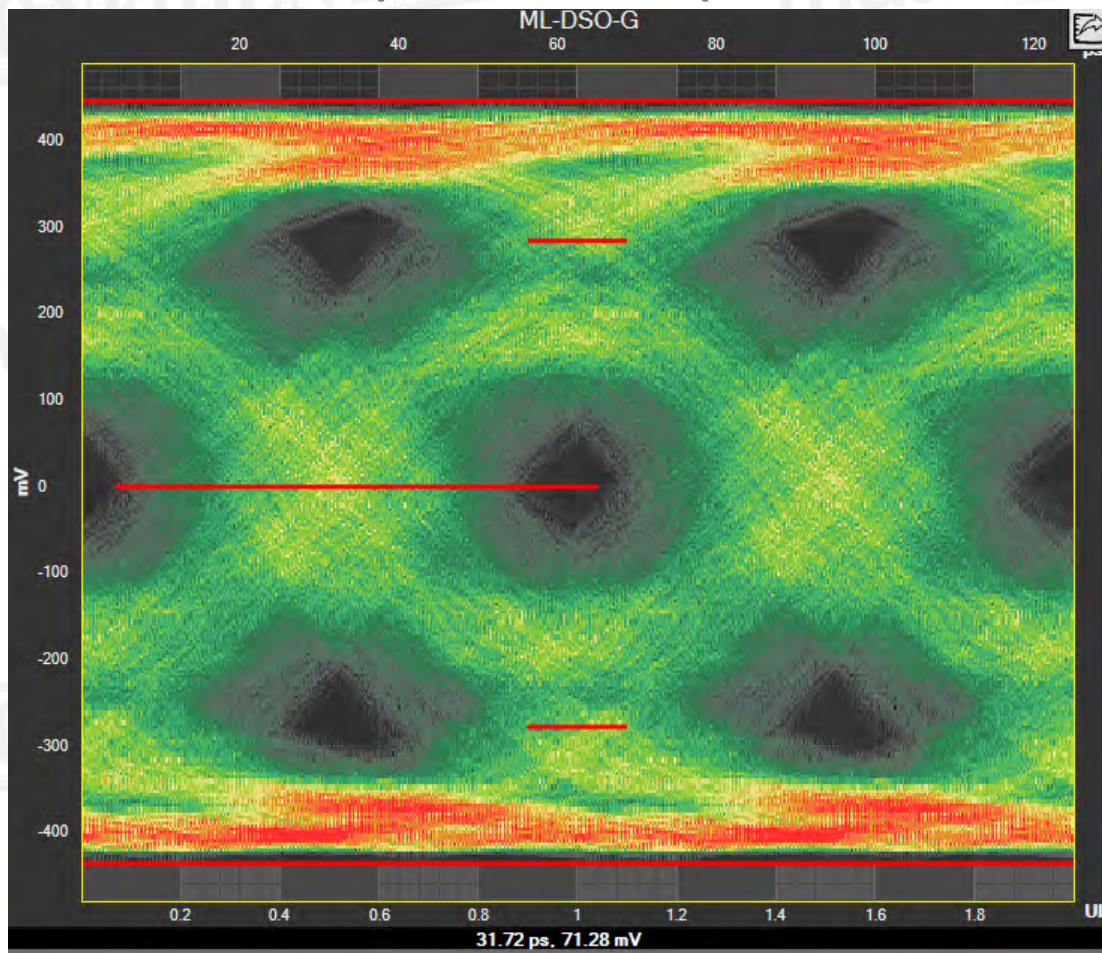
PRBS11 – SJ Amplitude 20 ps at **~60 MHz** and **~1 MHz** with ISI at **6dB**





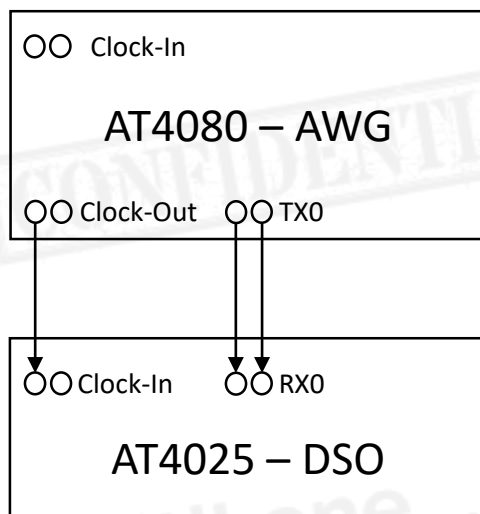
# PCIe Gen4 16Gbps – SJ Jitter and ISI injection at Tx

PRBS11 – SJ Amplitude 20 ps at **~60 MHz** and **~4 MHz** with ISI at **6dB**



# PCIe Gen3 8Gbps – PRBS 9

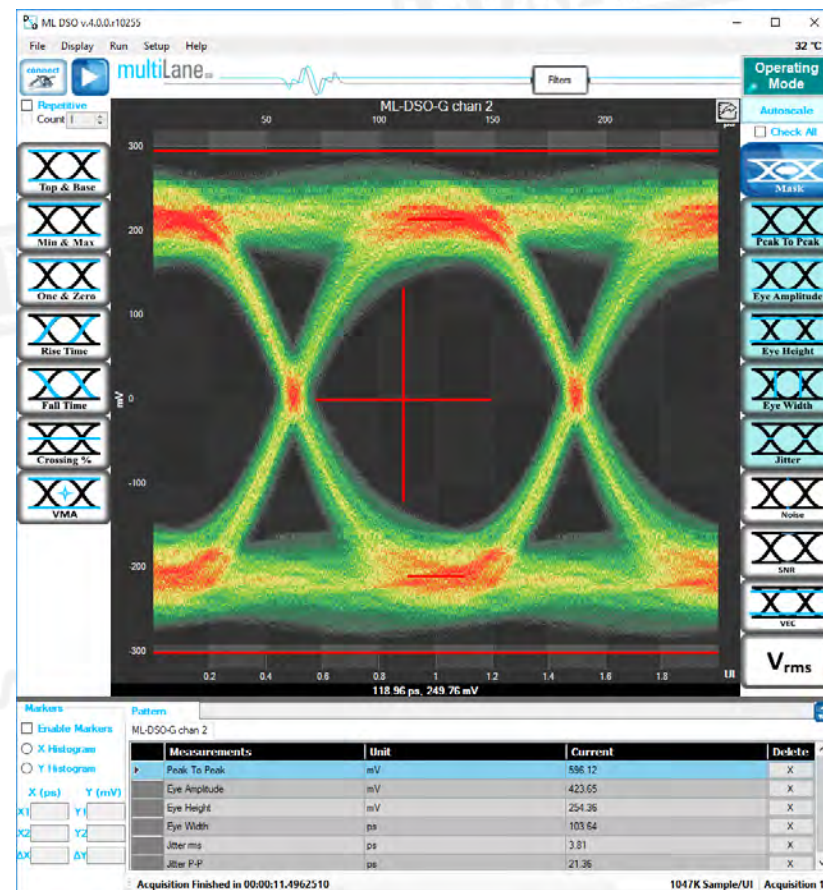
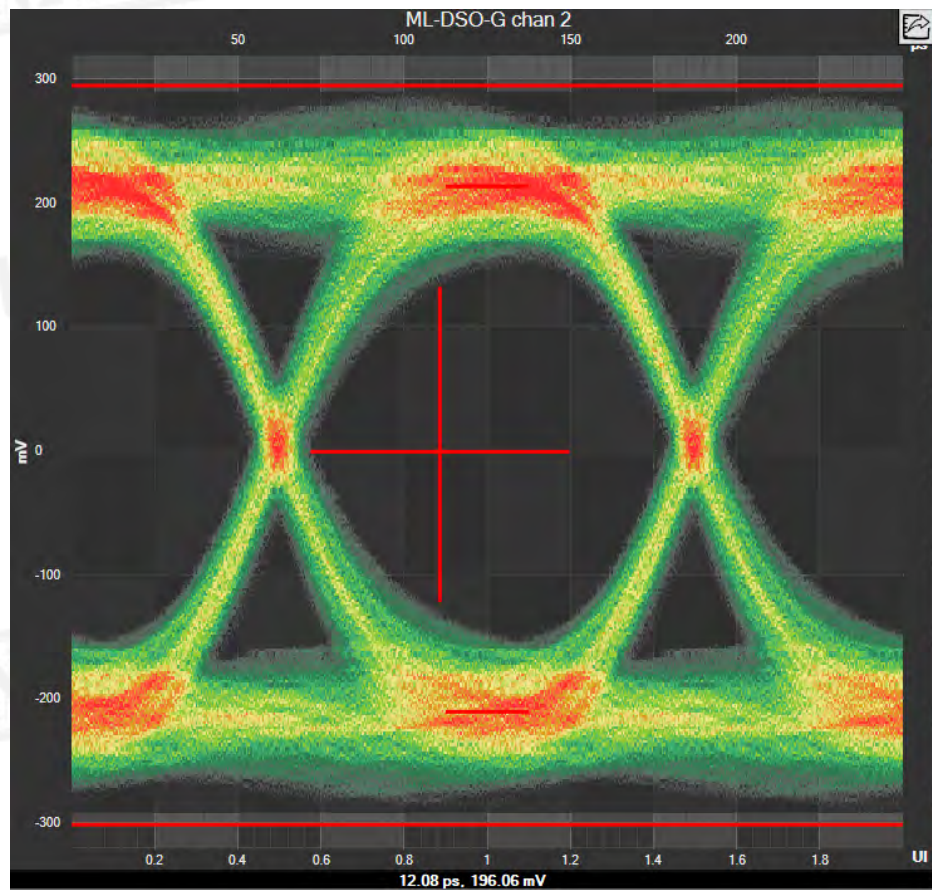
BUJ injection based on PN5 aggressor signal addition to emulate cross-talk





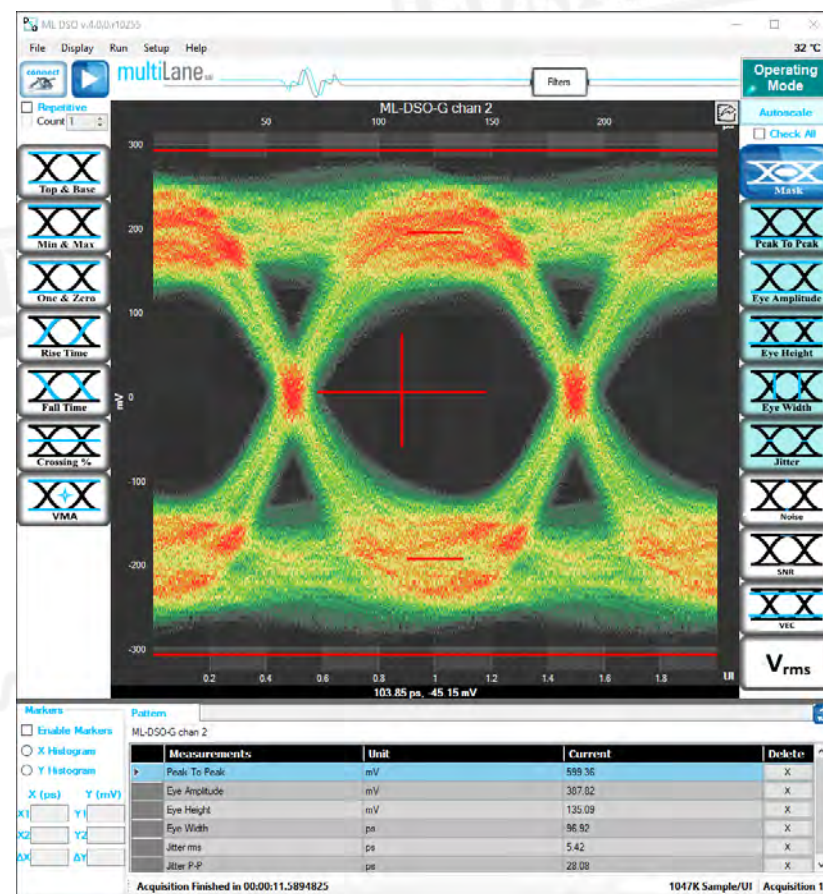
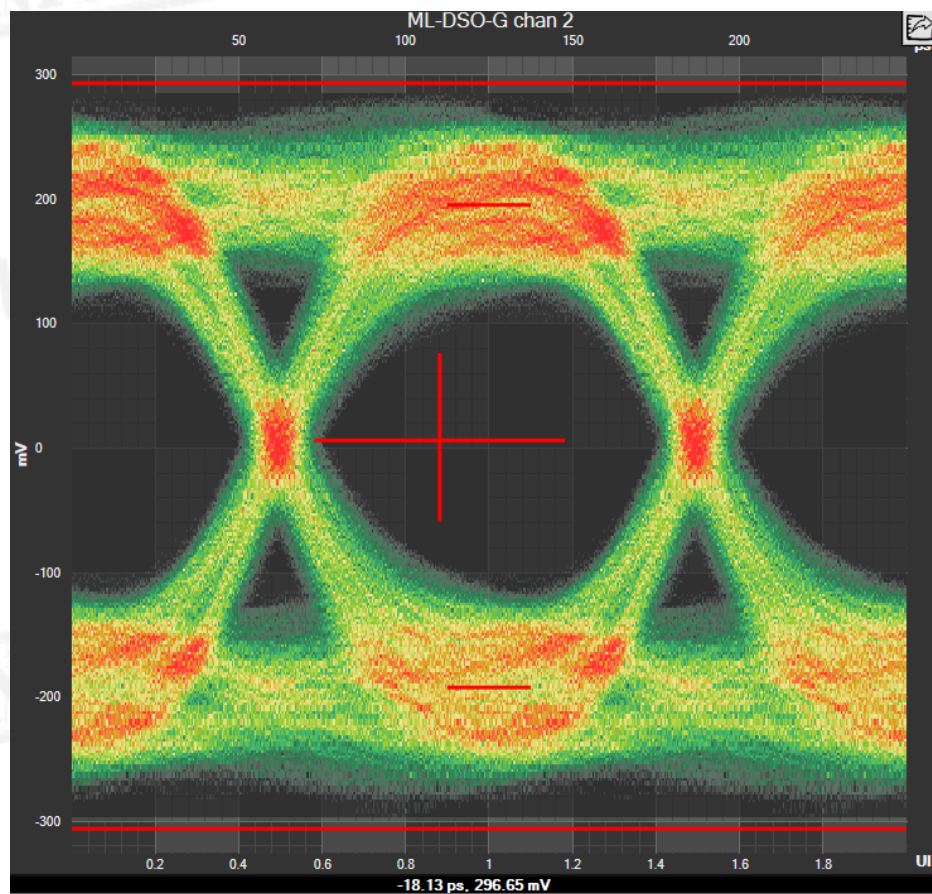
# PCIe Gen3 8Gbps – PRBS 9

BUJ injection based on **PN5 aggressor (0.1 SNR)** signal addition to emulate cross-talk



# PCIe Gen3 8Gbps – PRBS 9

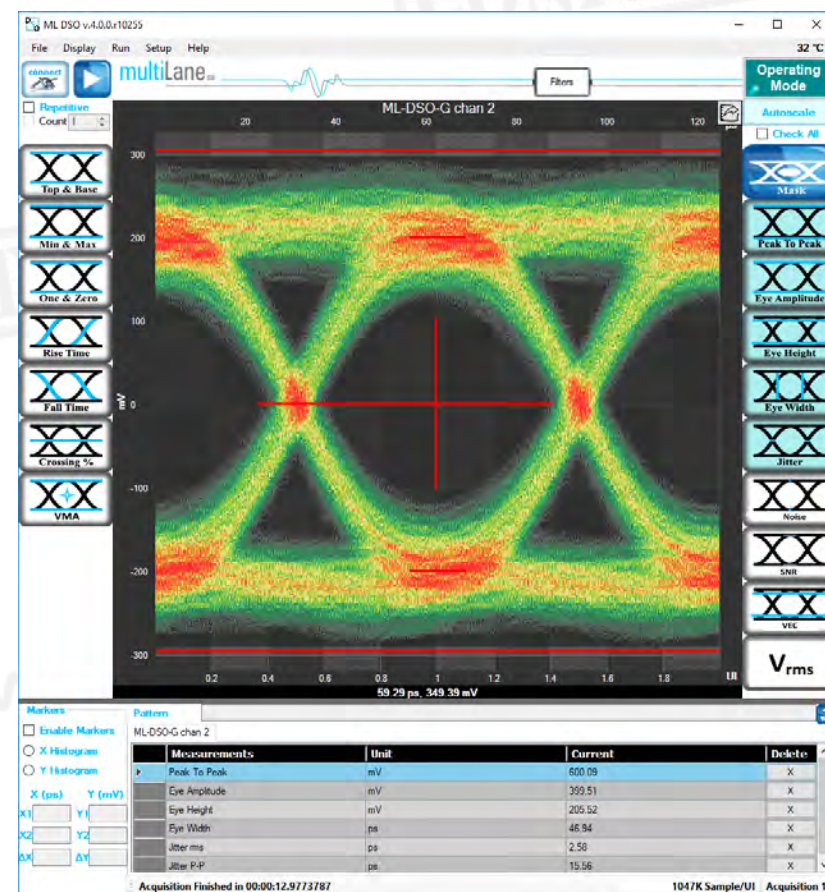
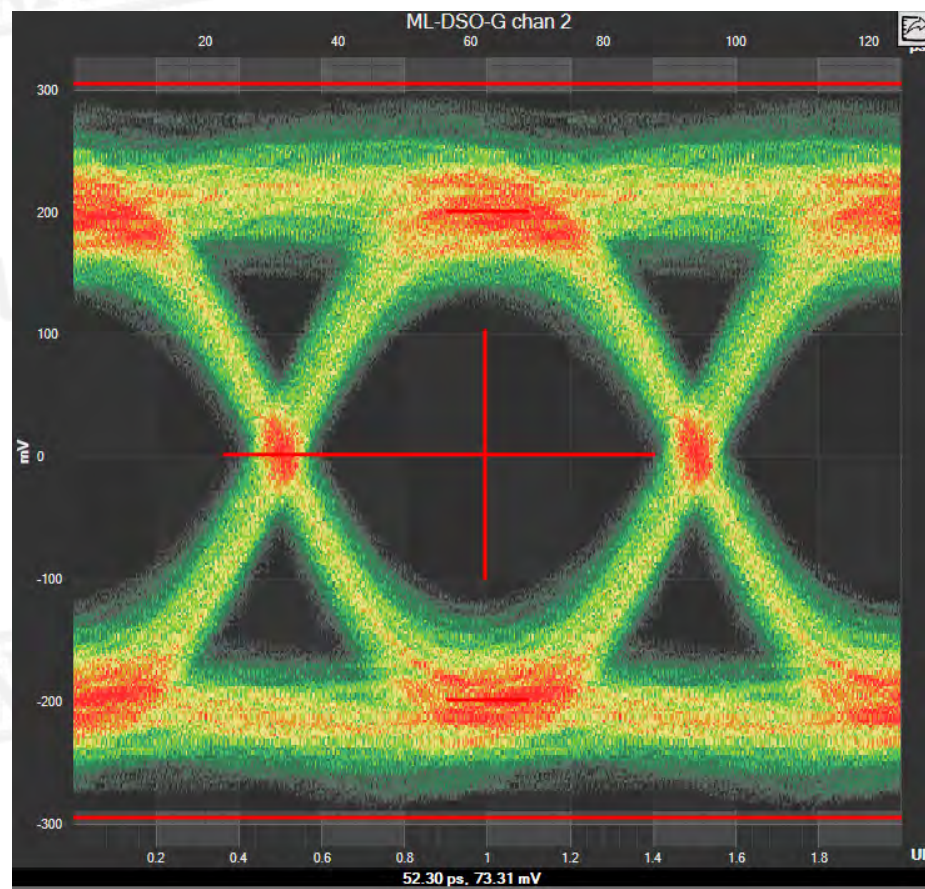
BUJ injection based on **PN5 aggressor (0.2 SNR)** signal addition to emulate cross-talk





# PCIe Gen4 16Gbps – PRBS 9

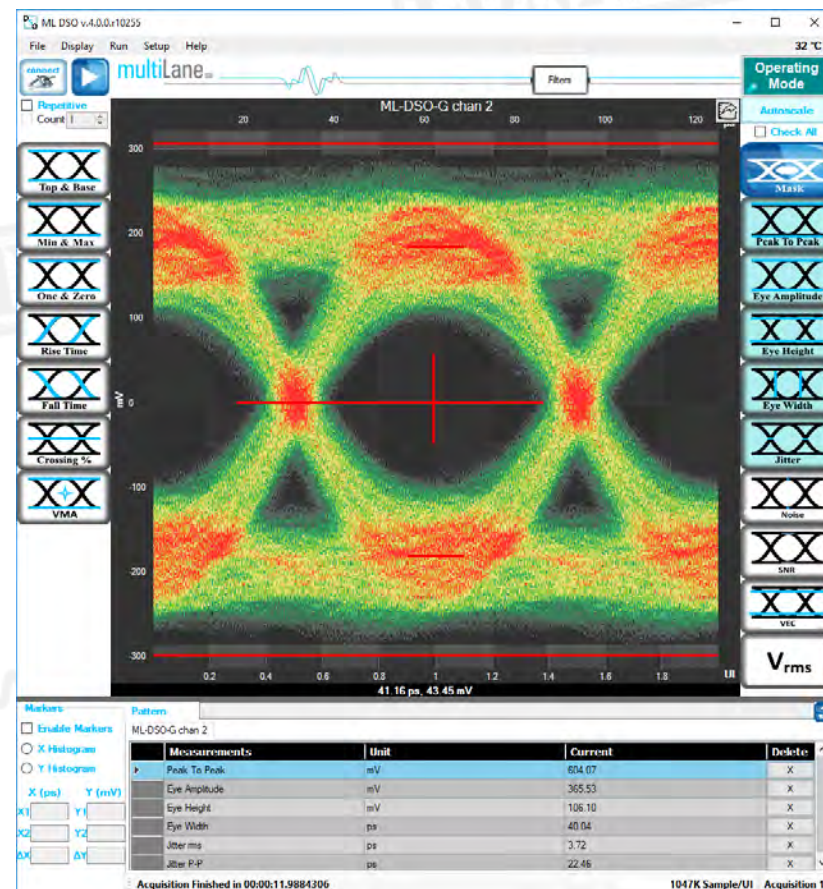
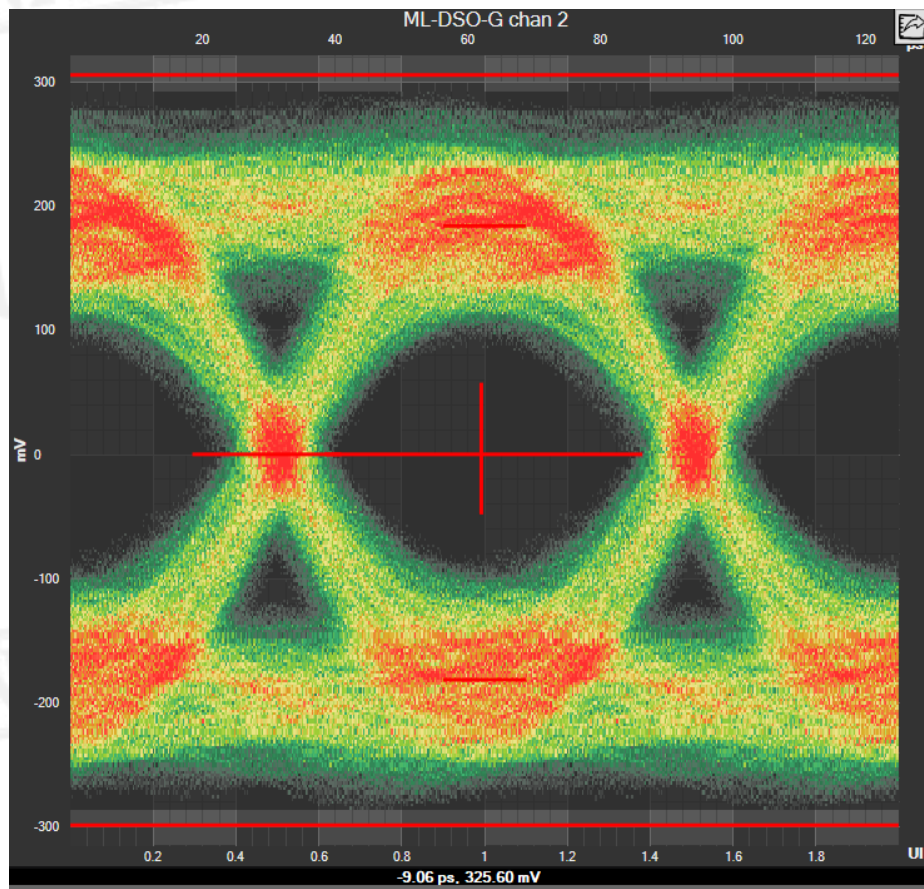
BUJ injection based on **PN5 aggressor (0.1 SNR)** signal addition to emulate cross-talk





# PCIe Gen4 16Gbps – PRBS 9

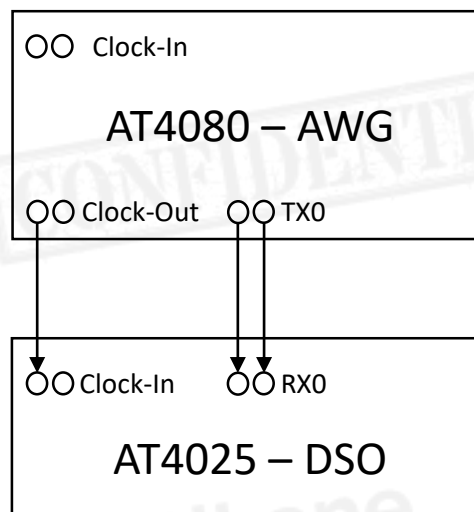
BUJ injection based on **PN5 aggressor (0.2 SNR)** signal addition to emulate cross-talk





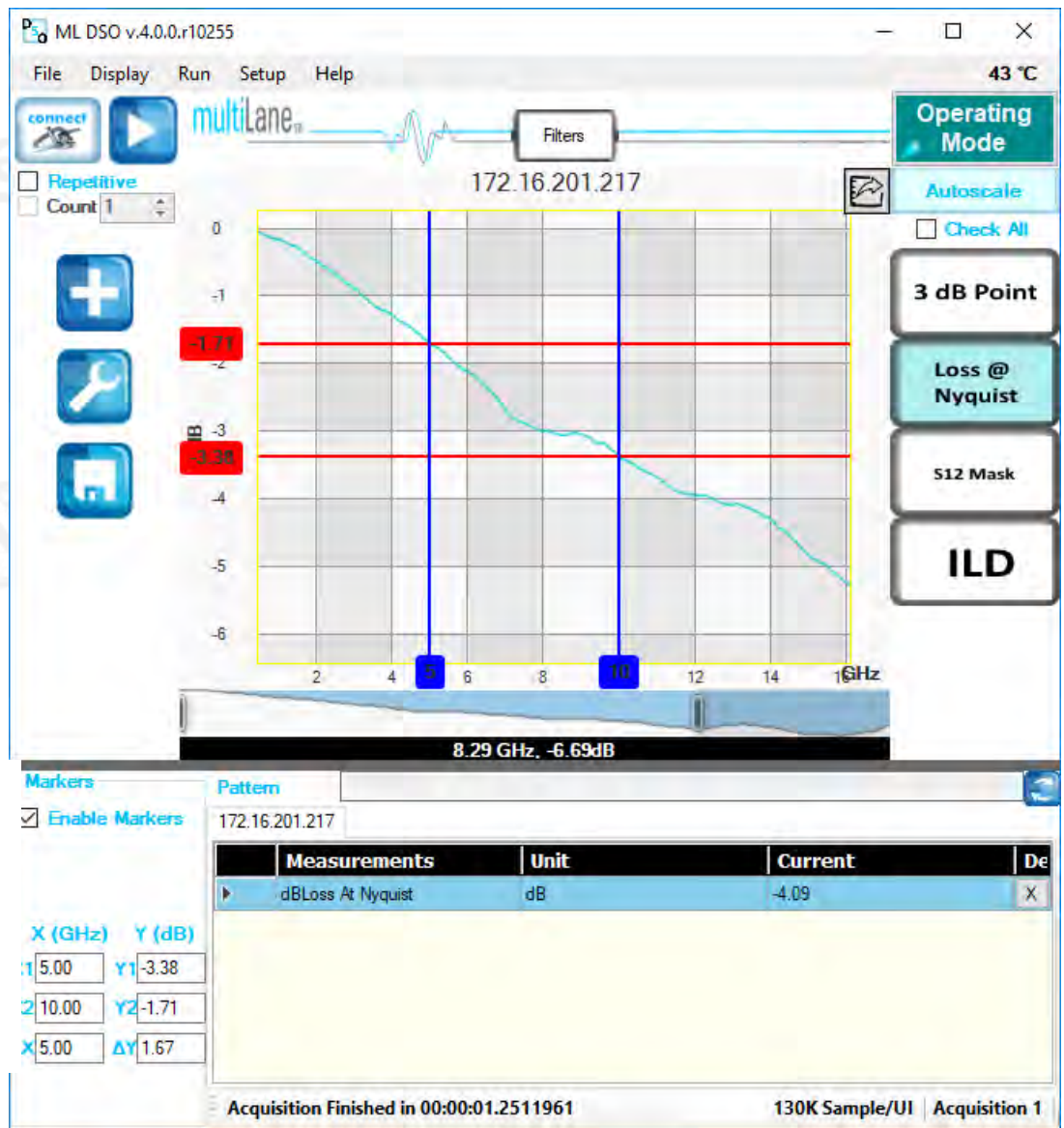
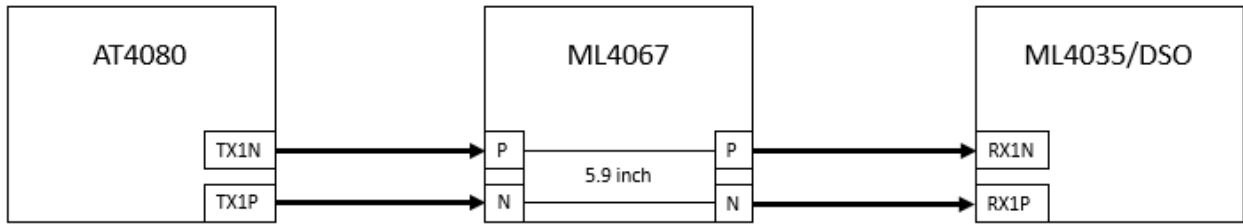
# PCIe Gen4 16Gbps – PRBS 7

De-embedding s-parameters by applying customized patterns after pre-processing



# 4080 Product

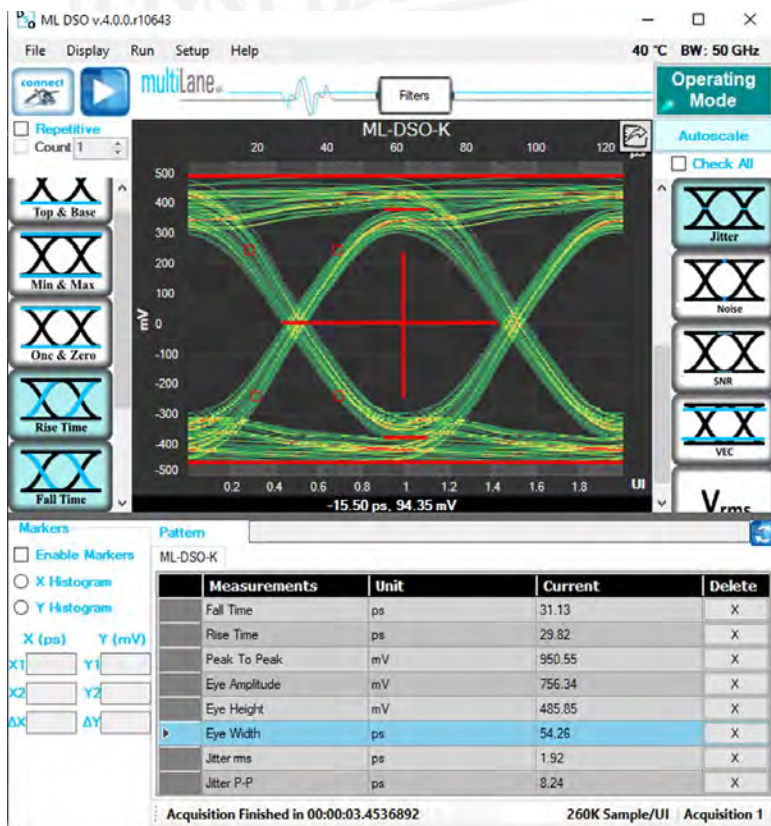
Insertion Loss addition using ML4067 (5.9 inches) and De-embedding



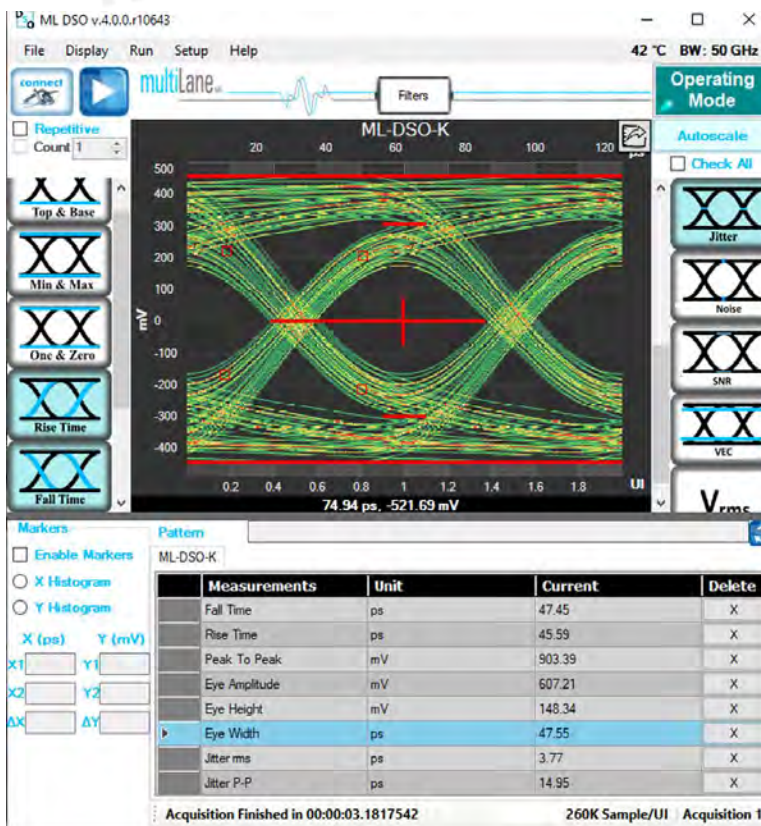


# 4080 Product

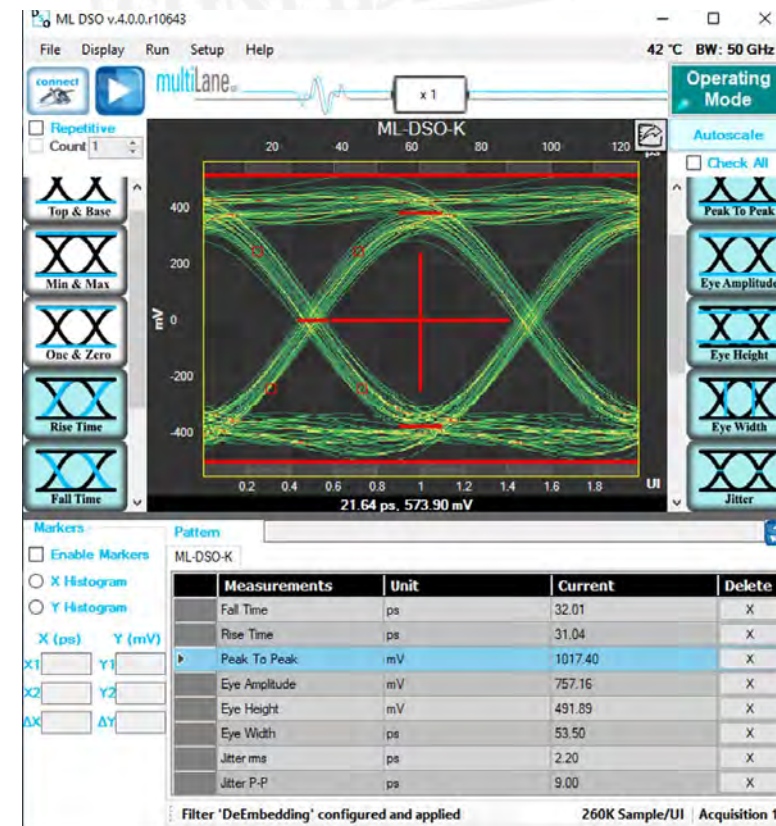
## Insertion Loss addition using ML4067 (5.9 inches) and De-embedding



PRBS7 16 Gbps – Reference signal



PRBS7 16 Gbps with 5.9 inches



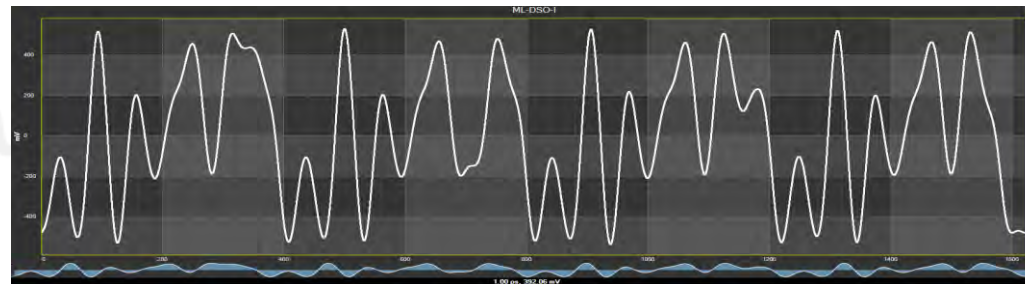
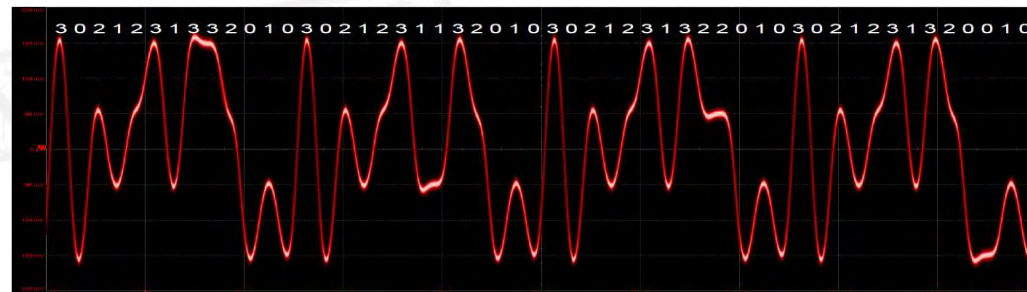
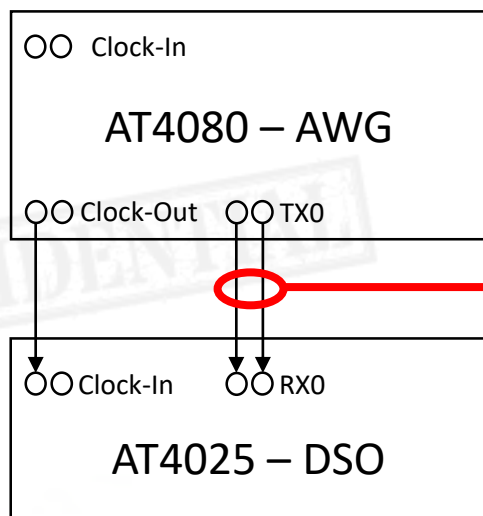
PRBS7 16 Gbps after De-embedding

# AT4080 – PCIe6 Compliance Testing

## PCIe 6.0 Jitter Measurement Pattern – Requirements

Pattern generation using AT4080

- Jitter Measurement Pattern is a 52 UI repeating sequence consisting of 4 sets of 13 UI per set
- Covers all 12 level transitions
- 12 transitions \* 4 sets = 48 edge transitions



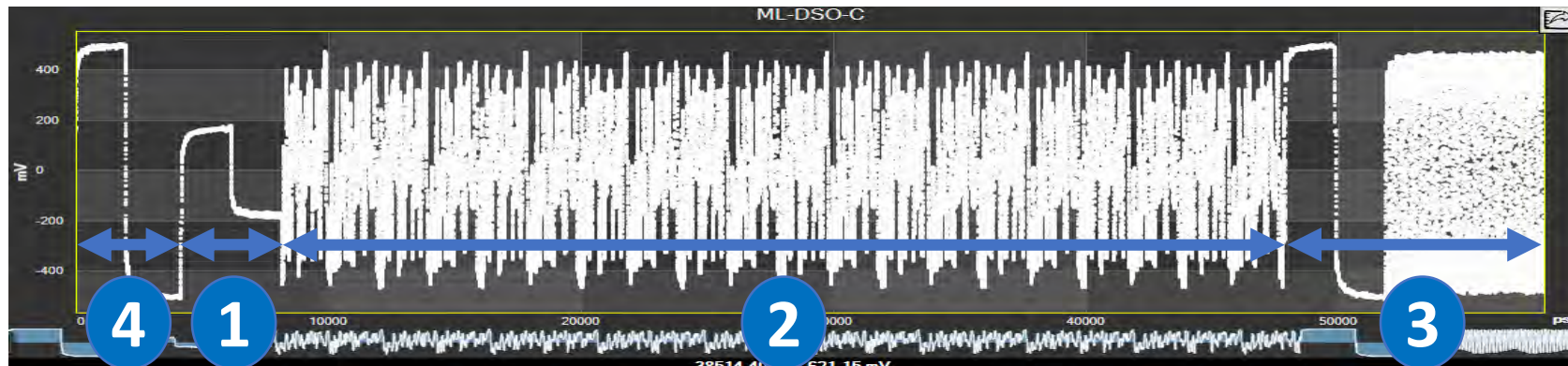


# AT4080 – PCIe6 Compliance Testing

## PCIe 6.0 Compliance Pattern Generation – Requirements

- Step 1: 64 UI at Level 2 then 64 UI at Level 1
- Step 2: PRBS signal
- Step 3: 64 UI at Level 3, 64 UI at Level 0, then Clock Signal
- Step 4: 64 UI at Level 3 then 64 UI at Level 0

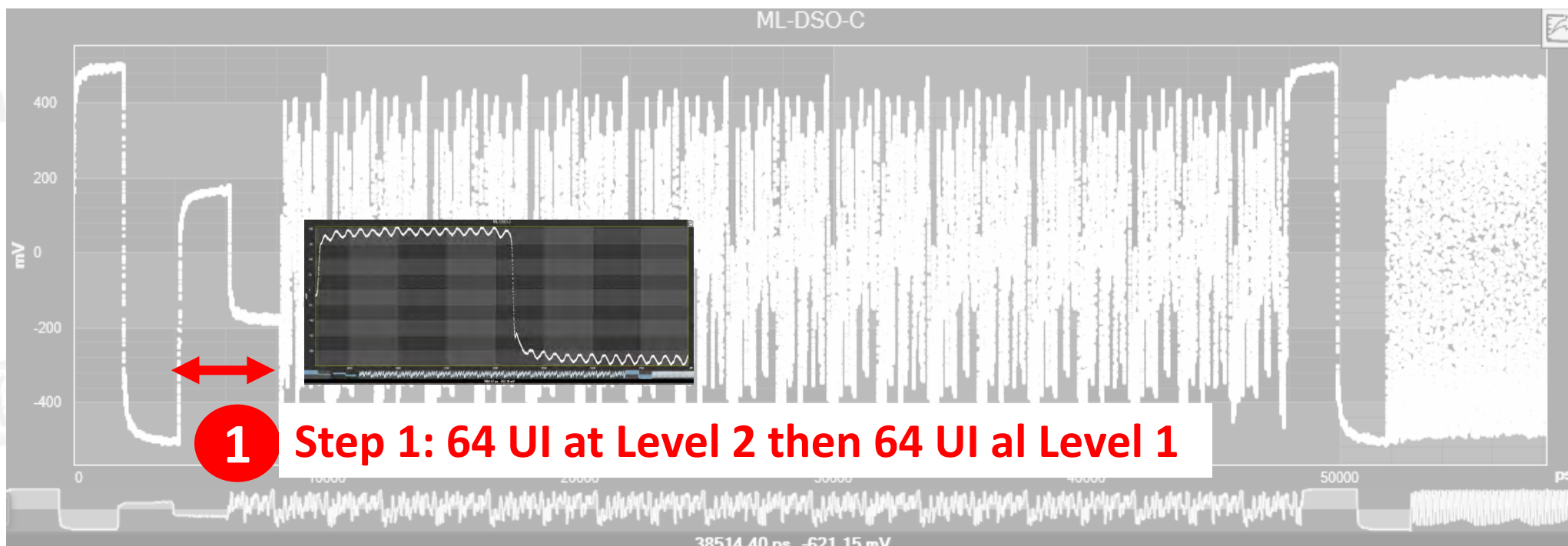
Pattern generation on AT4080 and acquisition on ML4035E



# AT4080 – PCIe6 Compliance Testing

PCIe 6.0 Compliance Pattern – Test results using ML products

Pattern generation on AT4080 and acquisition on ML4035E

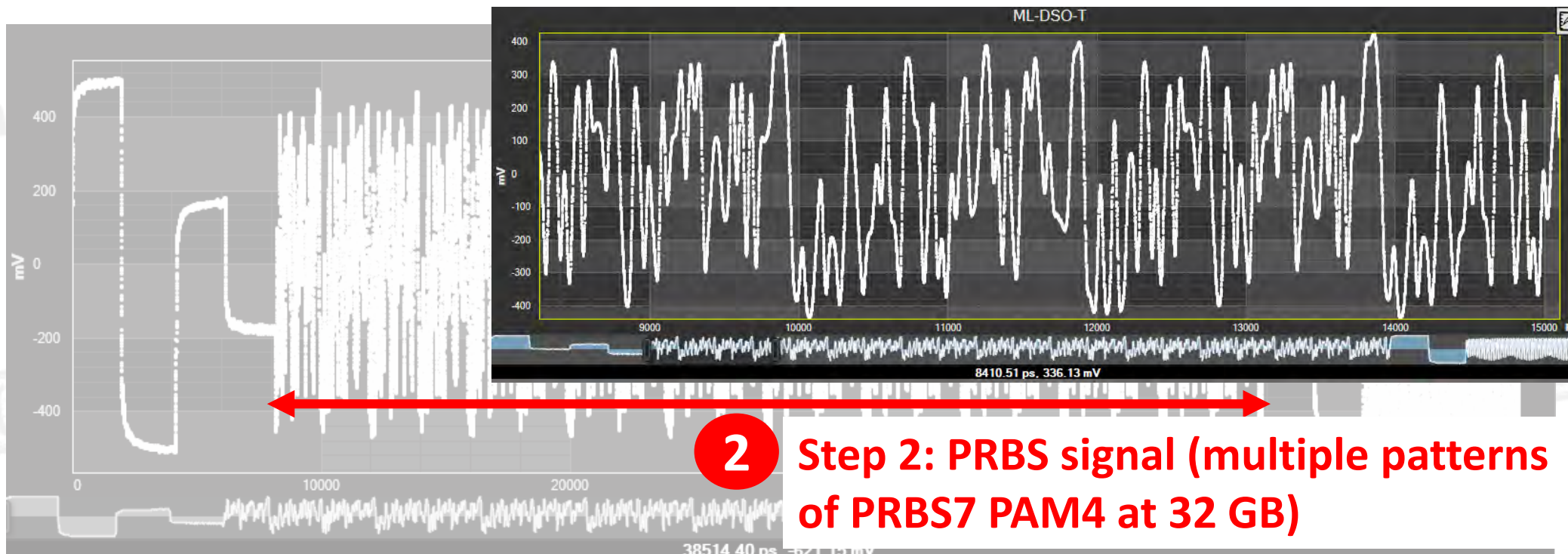




# AT4080 – PCIe6 Compliance Testing

PCIe 6.0 Compliance Pattern – Test results using ML products

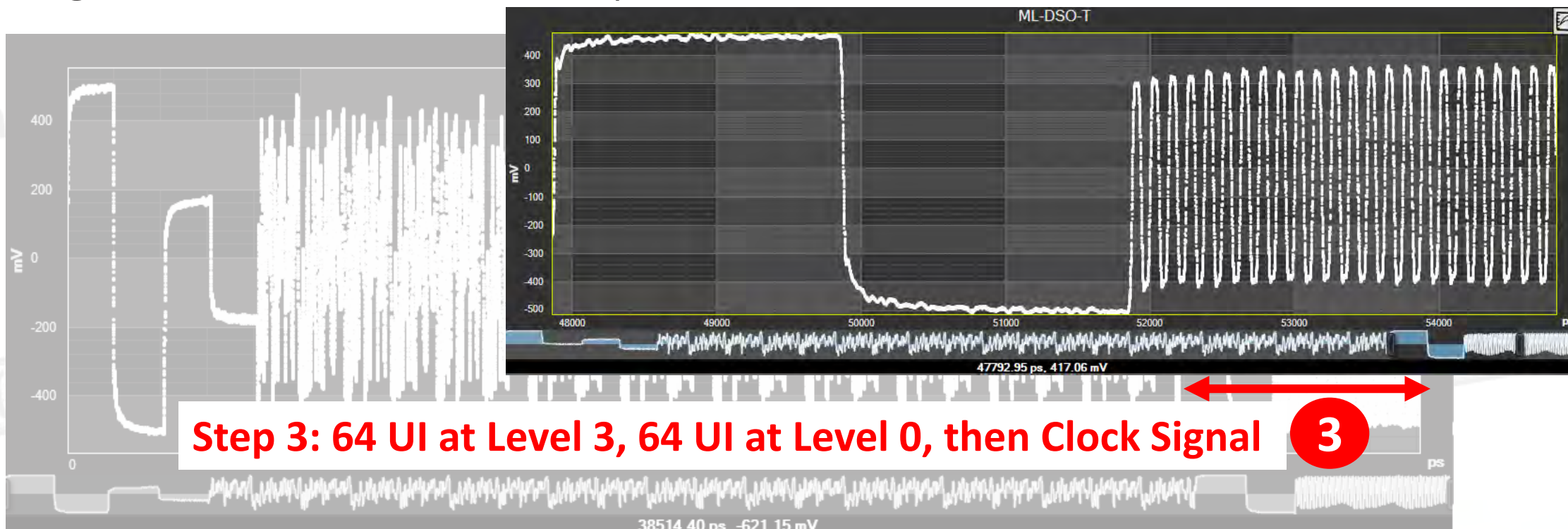
Pattern generation on AT4080 and acquisition on ML4035E



# AT4080 – PCIe6 Compliance Testing

PCIe 6.0 Compliance Pattern – Test results using ML products

Pattern generation on AT4080 and acquisition on ML4035E

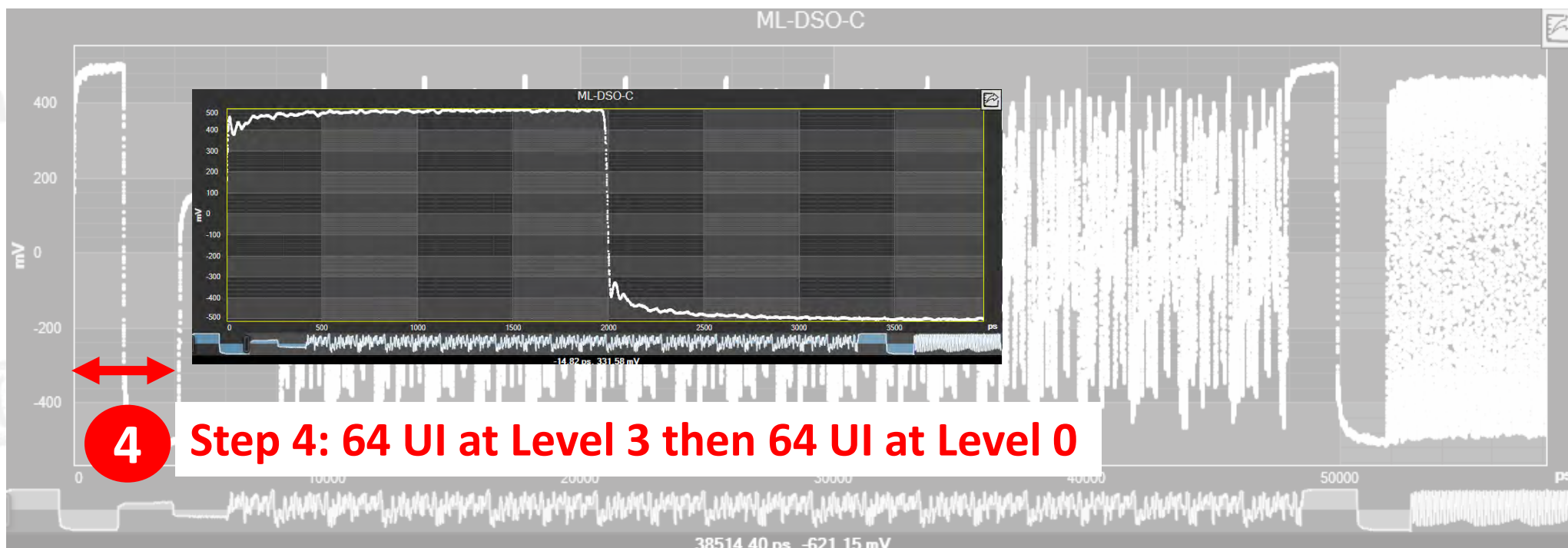




# AT4080 – PCIe6 Compliance Testing

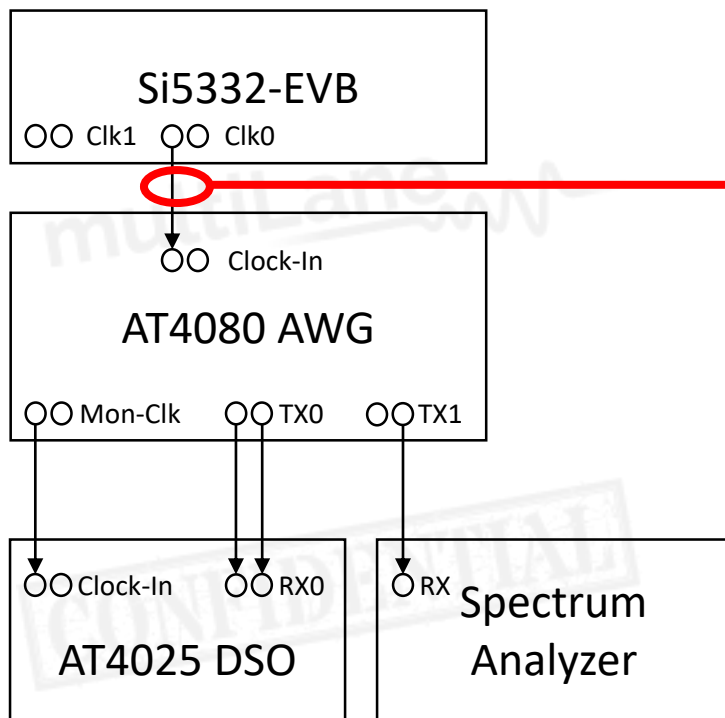
PCIe 6.0 Compliance Pattern – Test results using ML products

Pattern generation on AT4080 and acquisition on ML4035E

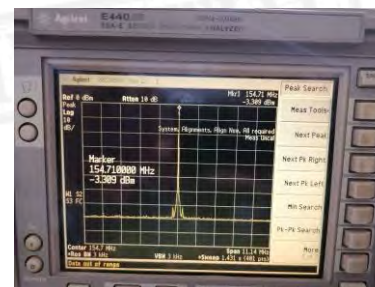


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability



SSC disabled

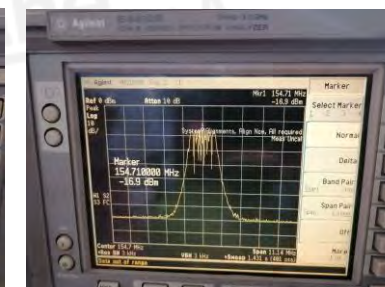


SSC enabled

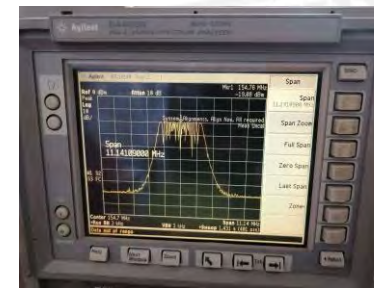
0.1%



0.5%



1%



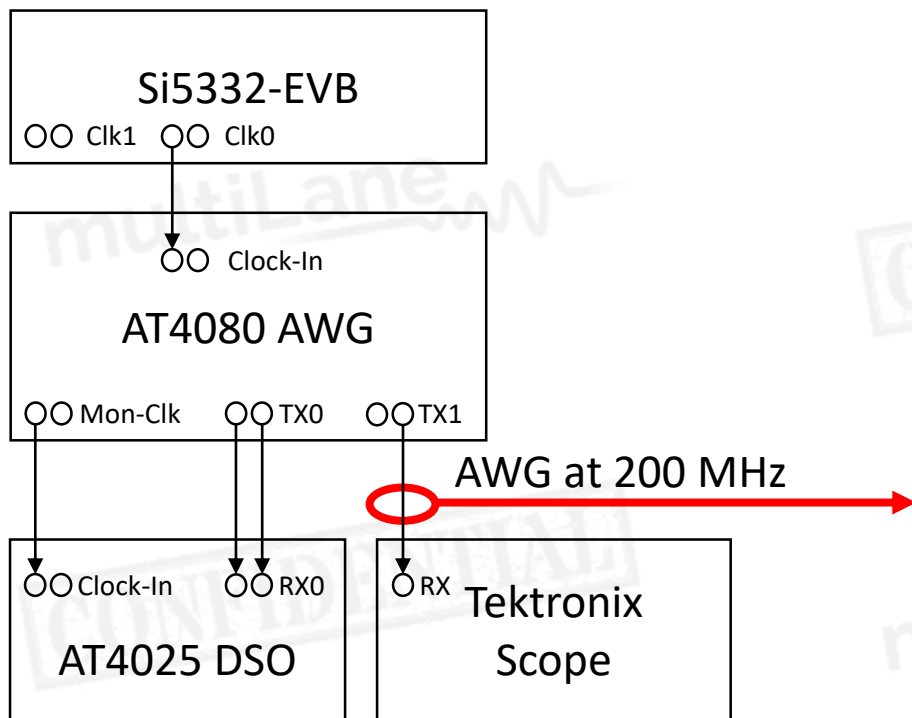
2.5%



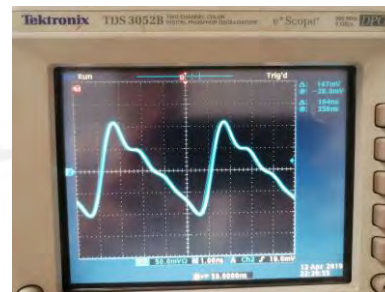
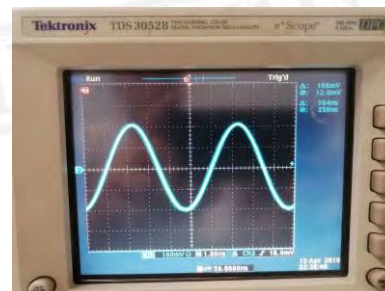


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability

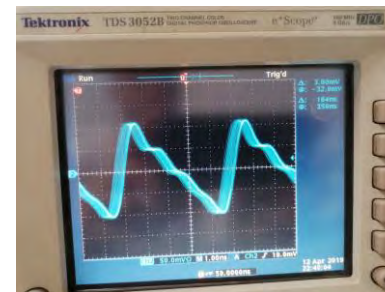
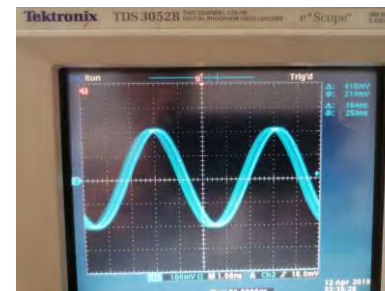


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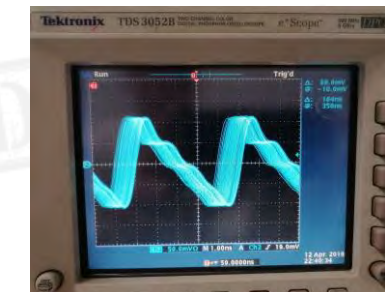
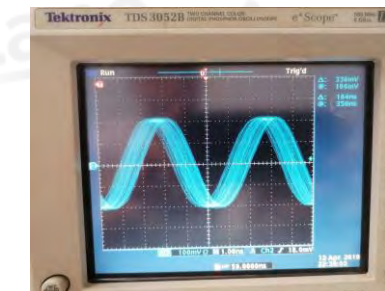


SSC enabled

Down Spread 2.5%

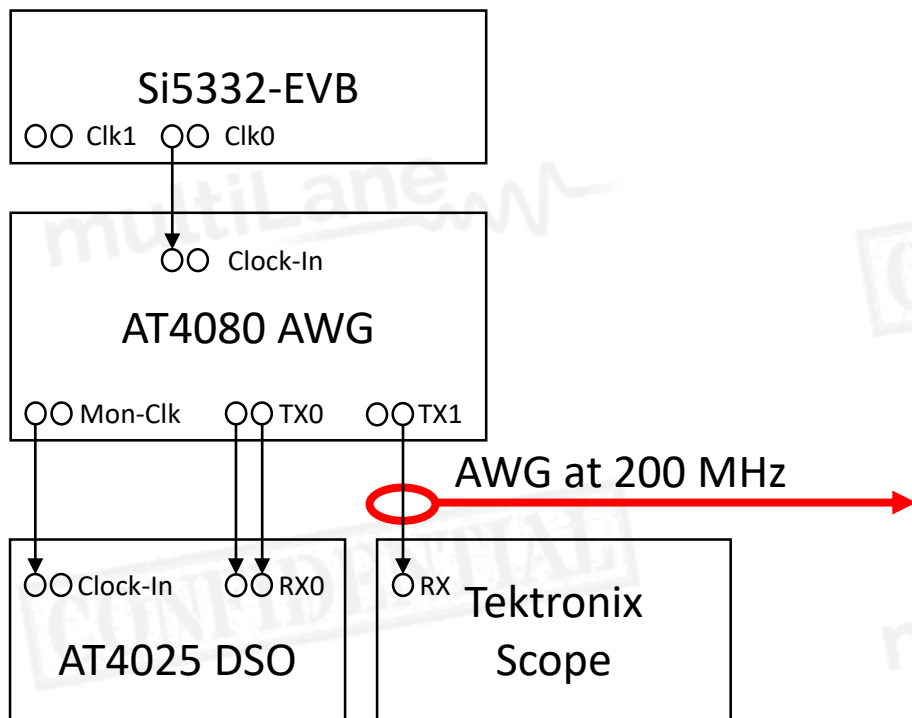


Center Spread 2.5%

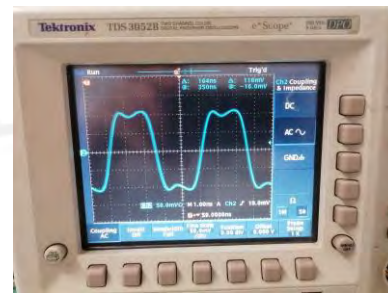
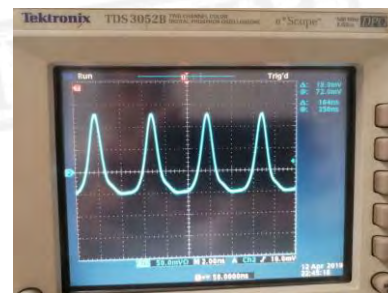


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability

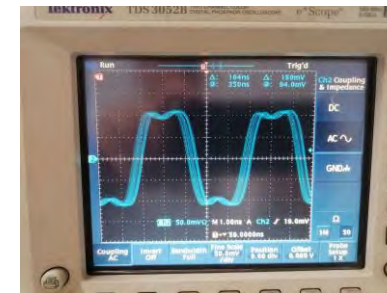
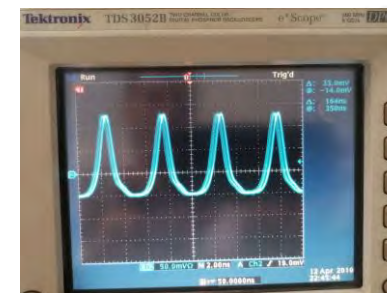


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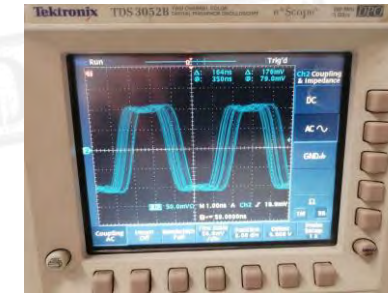
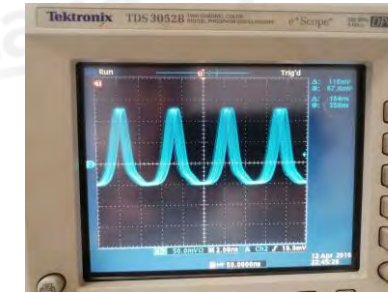


SSC enabled

Down Spread 2.5%



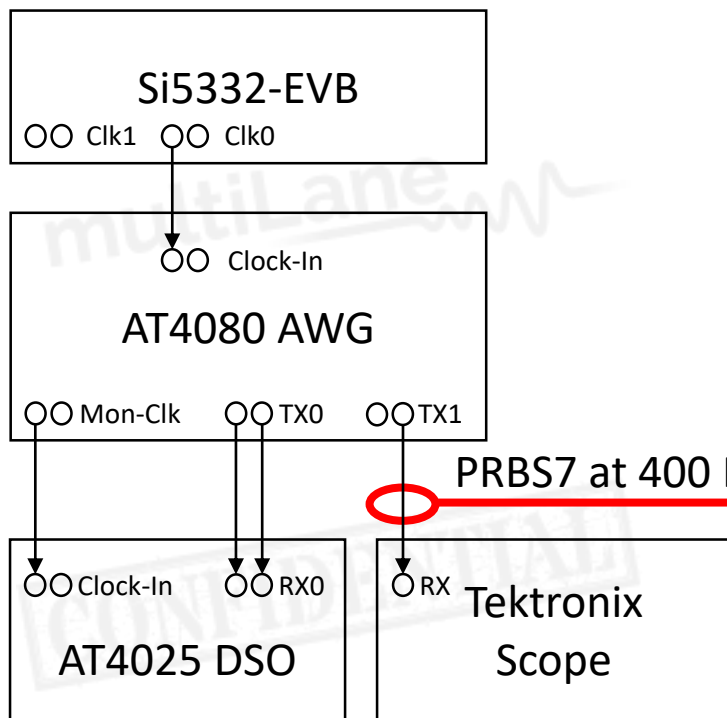
Center Spread 2.5%



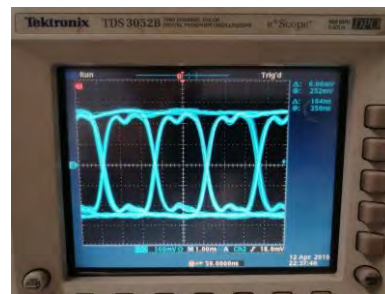


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability

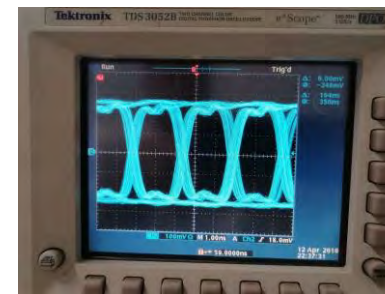


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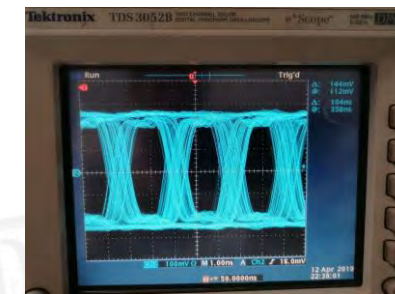


SSC enabled

Down Spread 2.5%

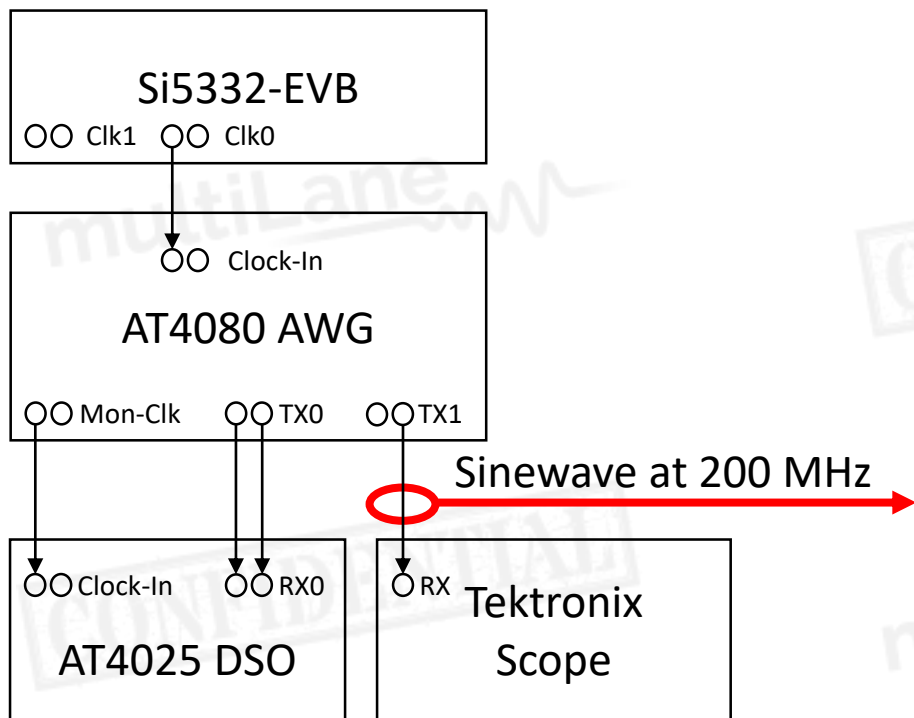


Center Spread 2.5%

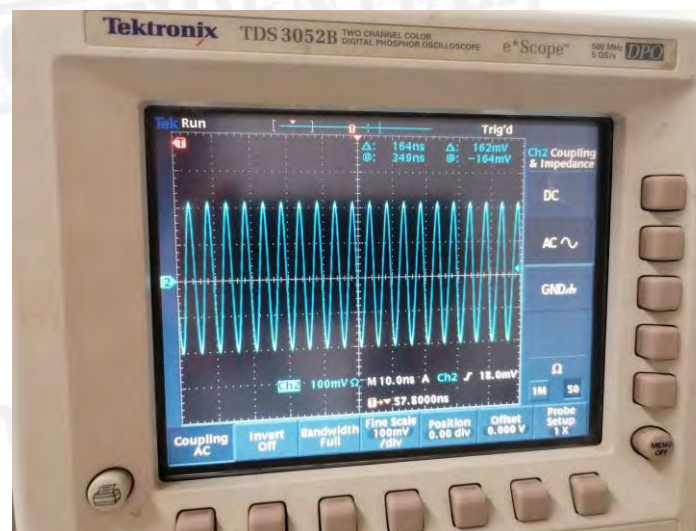


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability

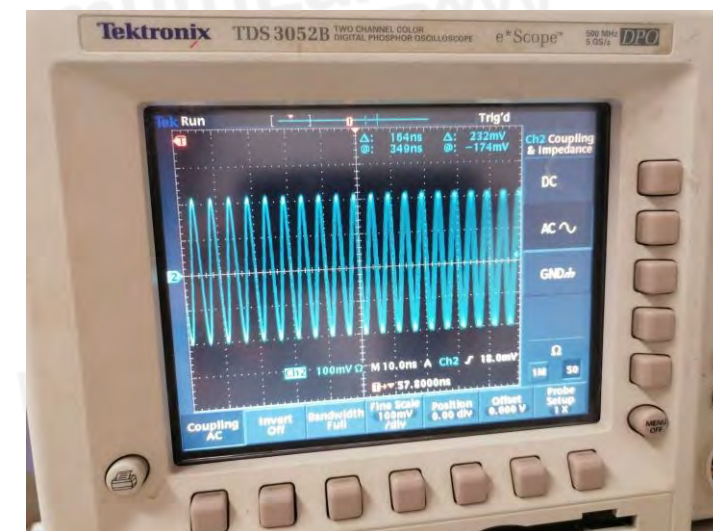


SSC disabled



SSC enabled

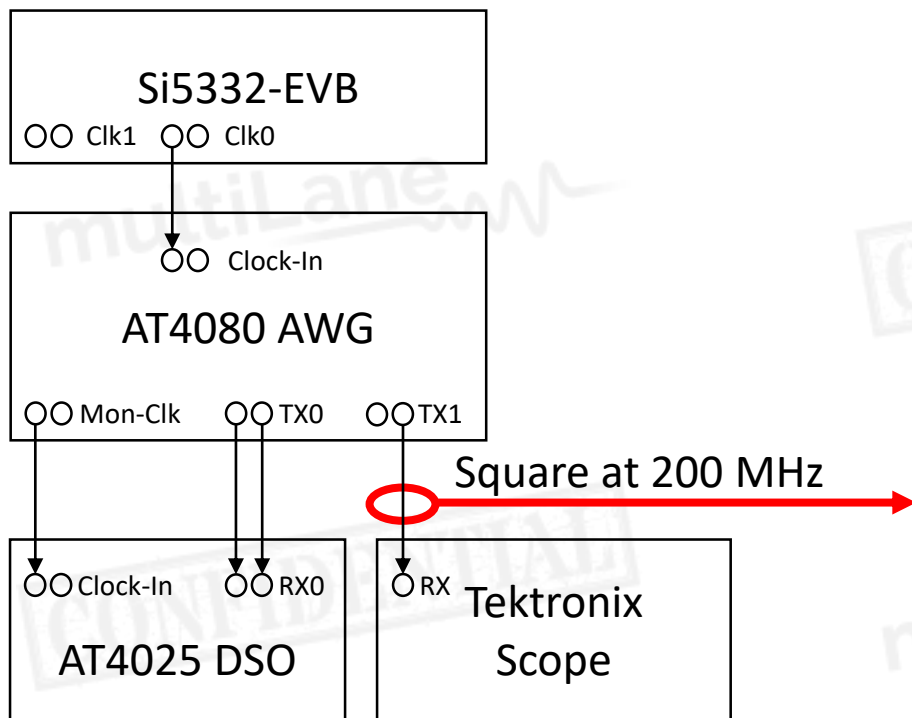
Center Spread 2.5%



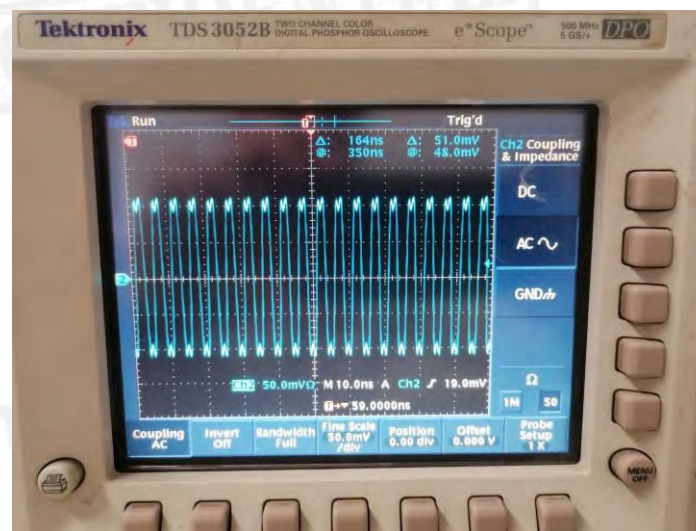


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability



SSC disabled



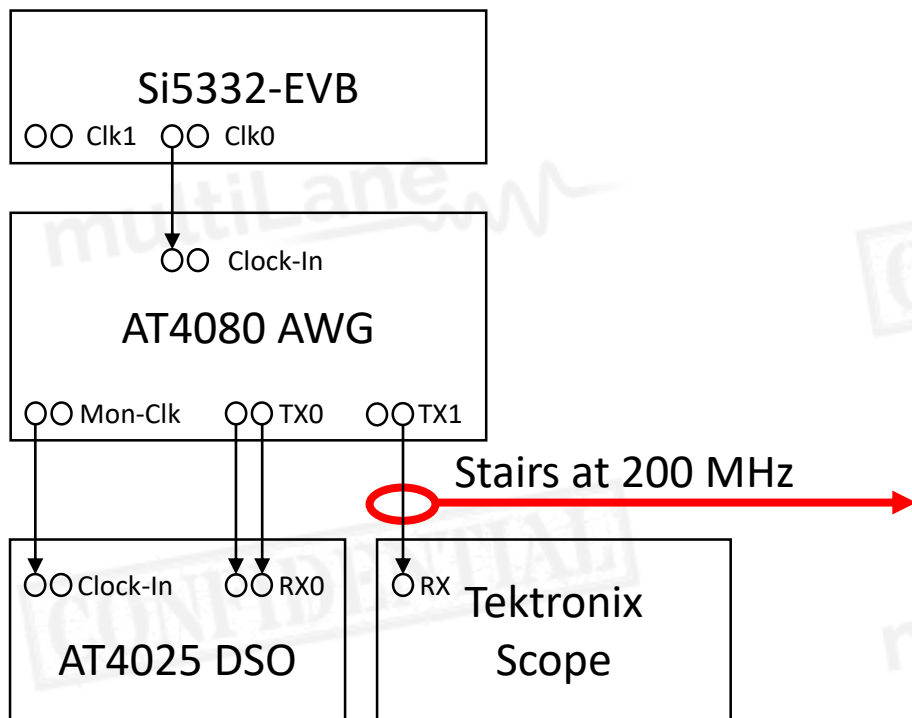
SSC enabled

Center Spread 2.5%

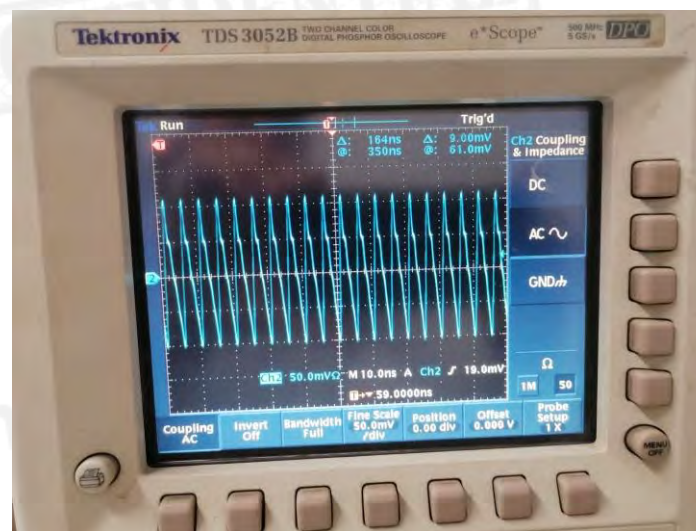


# AT4080 – SSC Clock

Generation of external reference clock from Si5332-EVB with SSC capability

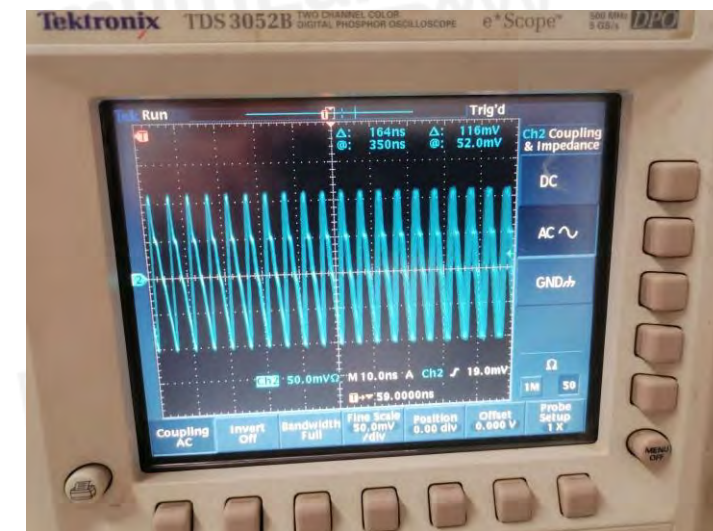


SSC disabled



SSC enabled

Center Spread 2.5%

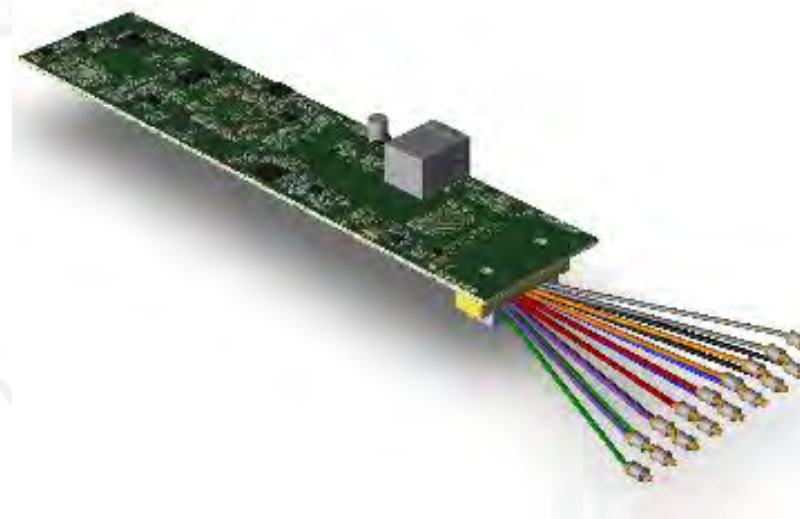
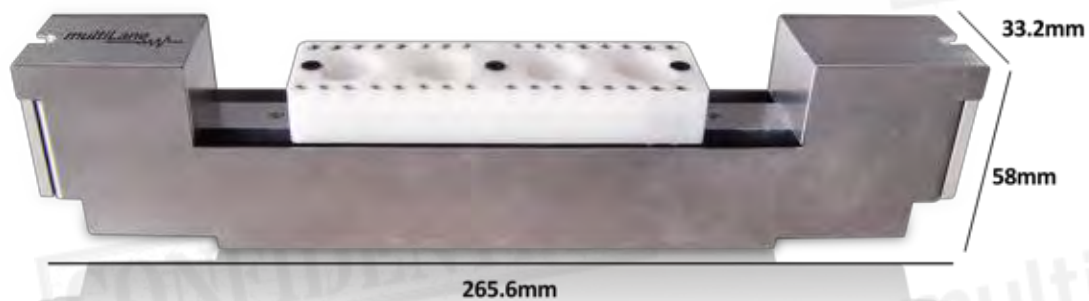




# 4080 Mechanical Overview

Available as AT4080, SL4080 and ML4080

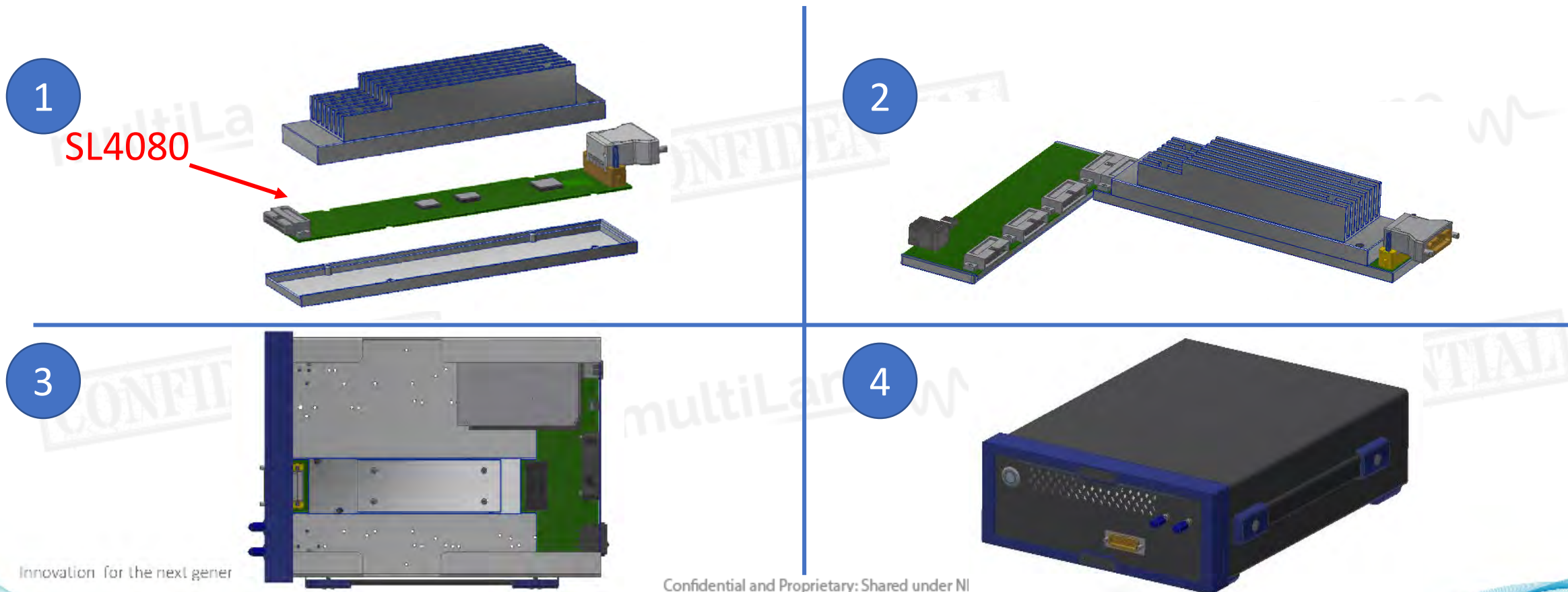
- AT4080: customized to fit and function inside an Advantest HSIO test head extender. One cassette can host up to 2xAT4080
- SL4080: customized to fit on a backplane on the side of the test head.



# 4080 Mechanical Overview

Available as AT4080, SL4080 and ML4080

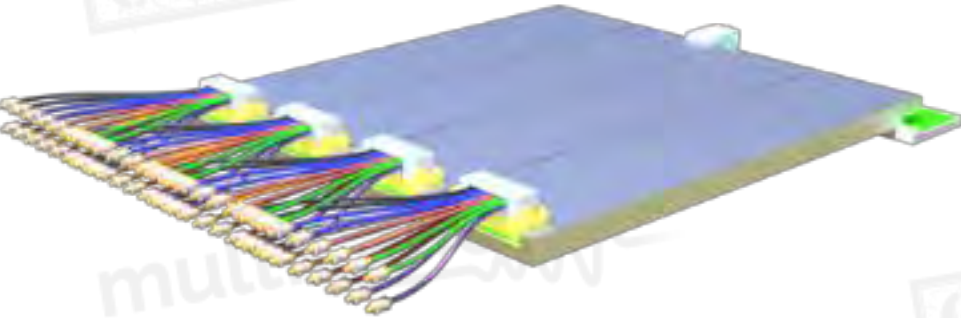
- ML4080: integrating the SL4080 into black box



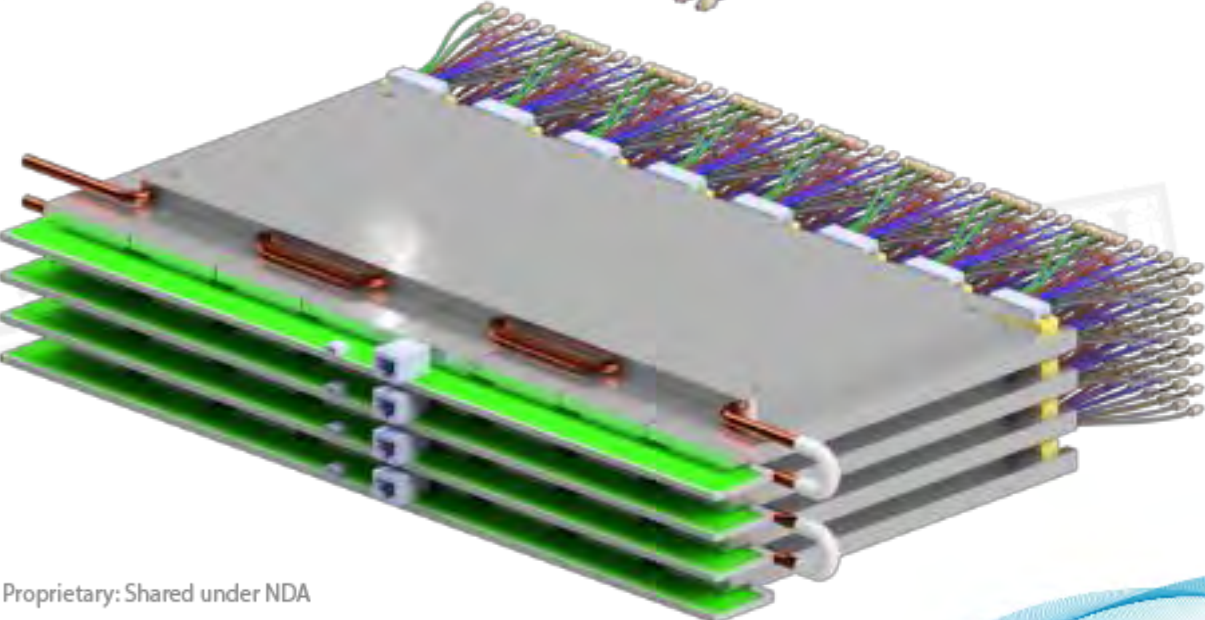
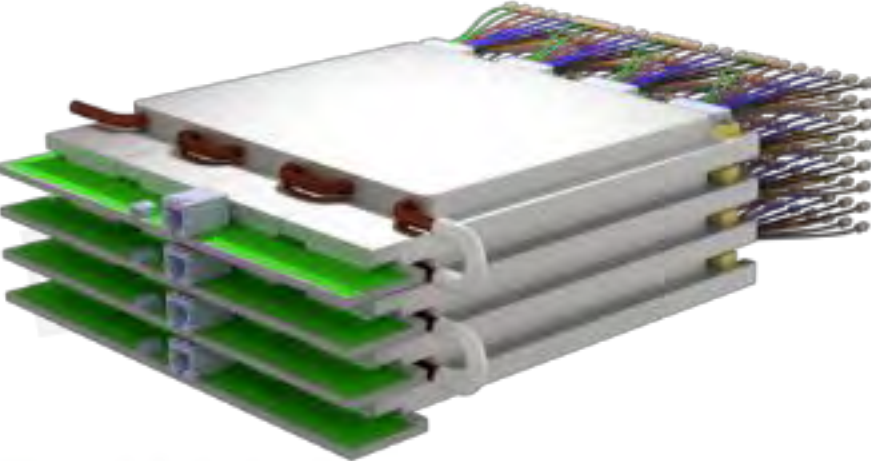
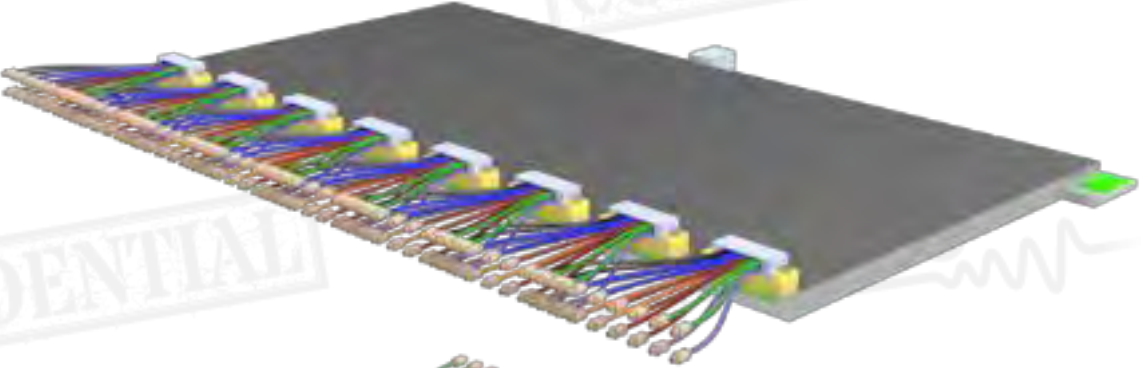


# Slices Overview

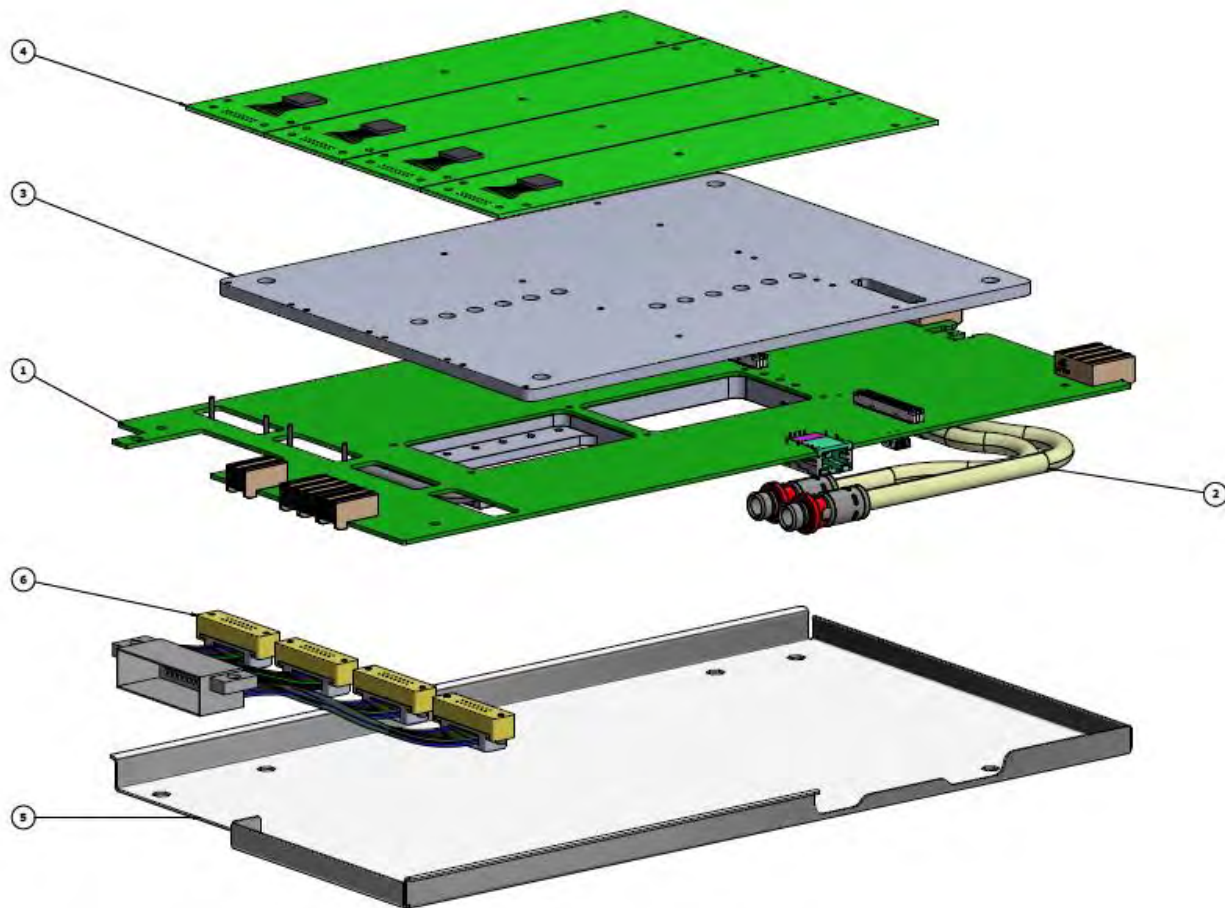
4 Modules



8 Modules



# SL4080 Slices on Carrier | Exploded View

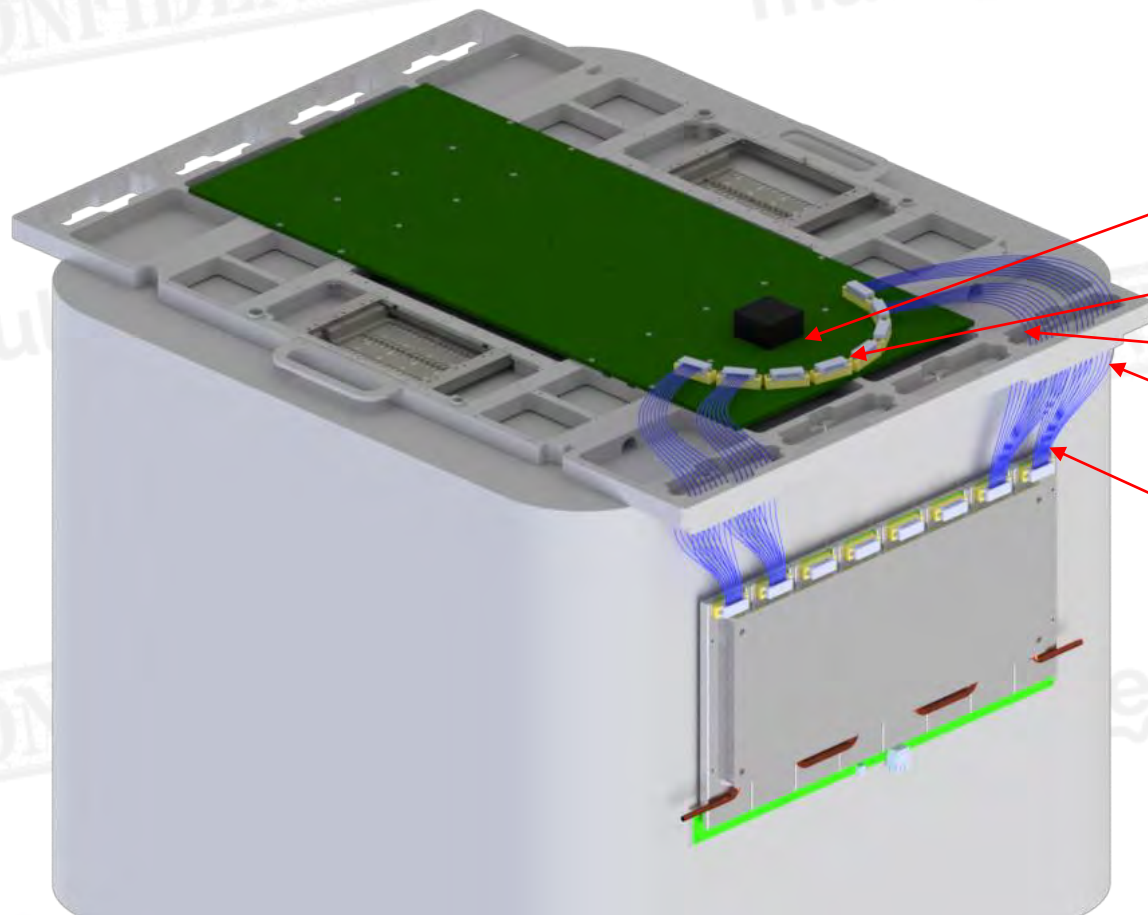


PARTS LIST			
ITEM	QTY	PART NUMBER	DESCRIPTION
1	1	Carrier-PCB	
2	1	HEAT SINK Customized	Customized Cooling Bar
3	1	heat transfer plate Option 2	
4	4	DC	Slice Cards
5	1	Cover	
6	4	TH28-RA To J10	2x8 Coax Cables to J10



# Integration on the Side of a Test Head

DUT on the side



Trace length ~3.5 inches (9 cm)

2x8 Connectors

TH28

RG405 cables 11 inches (48 cm)

Blind-mate interface  
SMPM

RG405 cables 5 inches (13 cm)

Estimated IL: ~ 2.5dB @28GHz with 0.79" cables



**Innovation for the next generation**

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